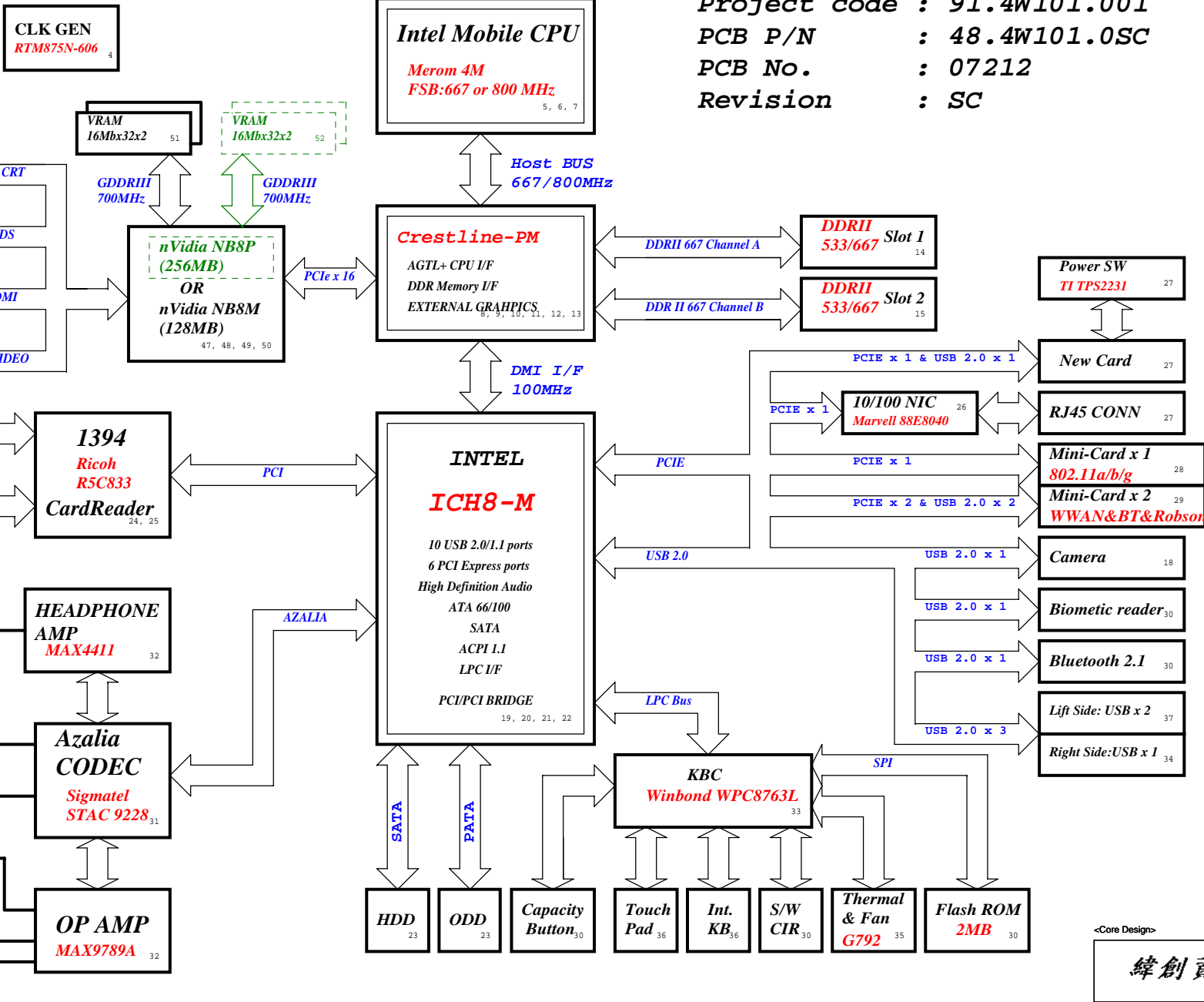


# Hawke Intel Discrete Block Diagram



Project code : 91.4W101.001  
PCB P/N : 48.4W101.0SC  
PCB No. : 07212  
Revision : SC

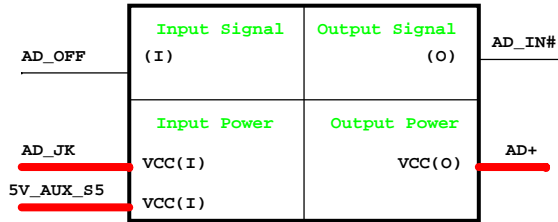
BATTERY CHARGER MAX8731A	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT
SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC TPS5117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
SYSTEM DC/DC TPS51100	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3
SYSTEM DC/DC RT9018	
INPUTS	OUTPUTS
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0
VGA DC/DC TPS5117	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0
CPU DC/DC ISL6262A	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
PCB LAYER	
L1:TOP	
L2:GND	
L3:Signal	
L4:Signal	
L5:VCC	
L6:Singal	
L7:GND	
L8:BOT	

<Core Design>

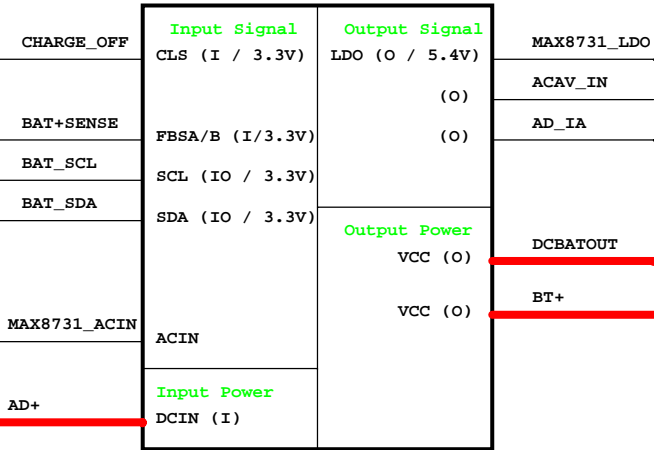
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System Block Diagram		
Size	Document Number	Rev
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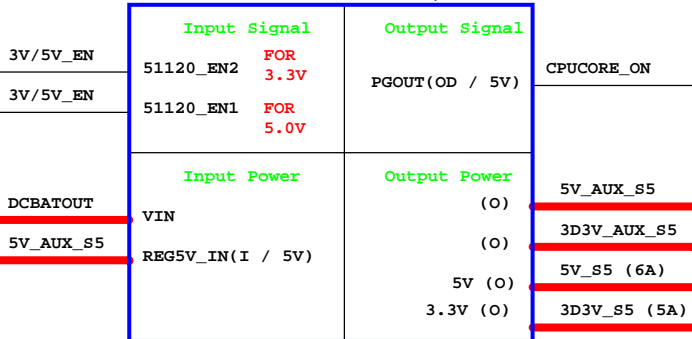
## Adapter



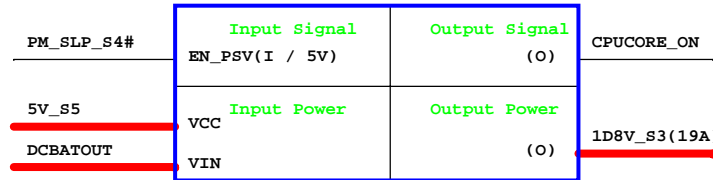
## Charger MAX8731A



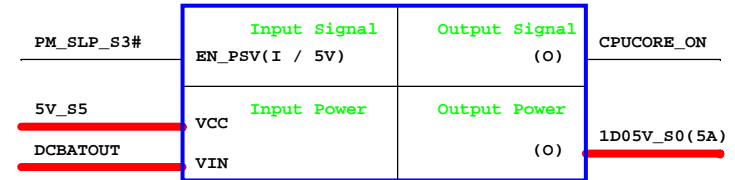
## TI TPS51120 3D3V/5V



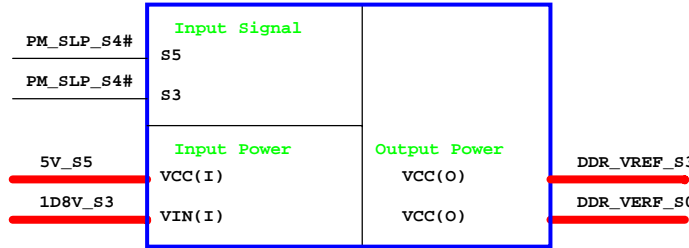
## TPS51117 1D8V



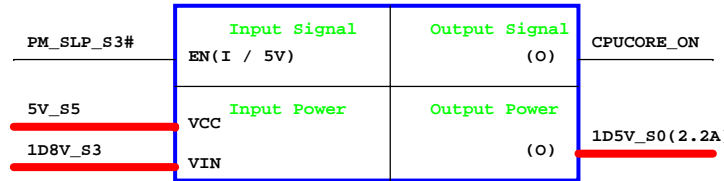
## TPS51117 1D05V



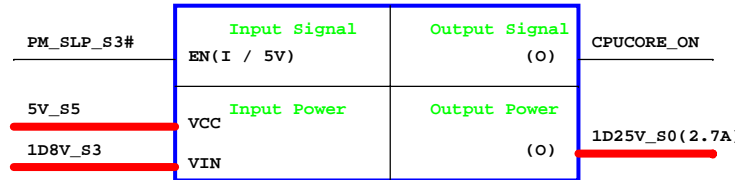
## TI TPS51100 0.9V/DDR\_VREF\_S3



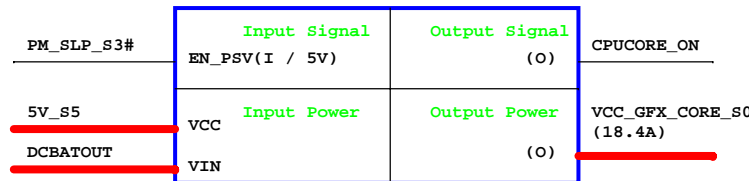
## RT9018A 1D5V



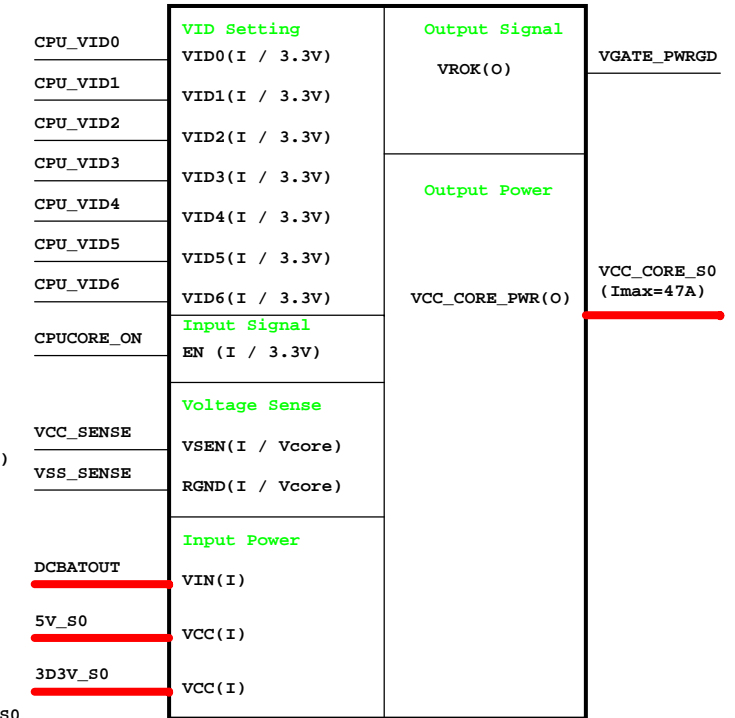
## RT9018A 1D25V



## TPS51117 VGA\_CORE



## ISL6262A CPU\_CORE



<Core Design>

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Title		
Power Block Diagram		
Size A3	Document Number	Rev
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## INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP_Tp3	AZ_DOUT_ICH	Description	
0	0	RSVD	
0	1	Enter XOR Chain	
1	0	Normal Operation(default)	
1	1	Set PCIE port cofig bit1	

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	
	high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

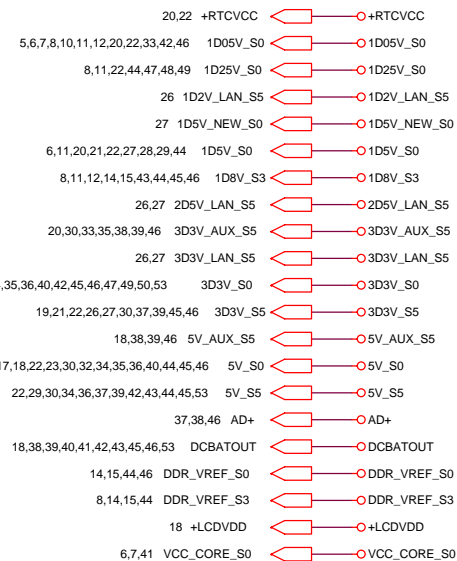
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

## INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CI_RST#	TBD



## PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

## USB TABLE

USB0	Ext Lift Side (Bottom)
USB1	Ext Lift Side (Top)
USB2	Ext Right Side
USB3	N/A
USB4	WWAN
USB5	Bluetooth
USB6	Camera
USB7	Biometric
USB8	Express Card
USB9	3rd mini card

## PCIE Routing

LANE1	10/100M Bit LOM
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN
LANE4	BT/UWB/Robson
LANE5	Express Card
LANE6	N/A

<Core Design>

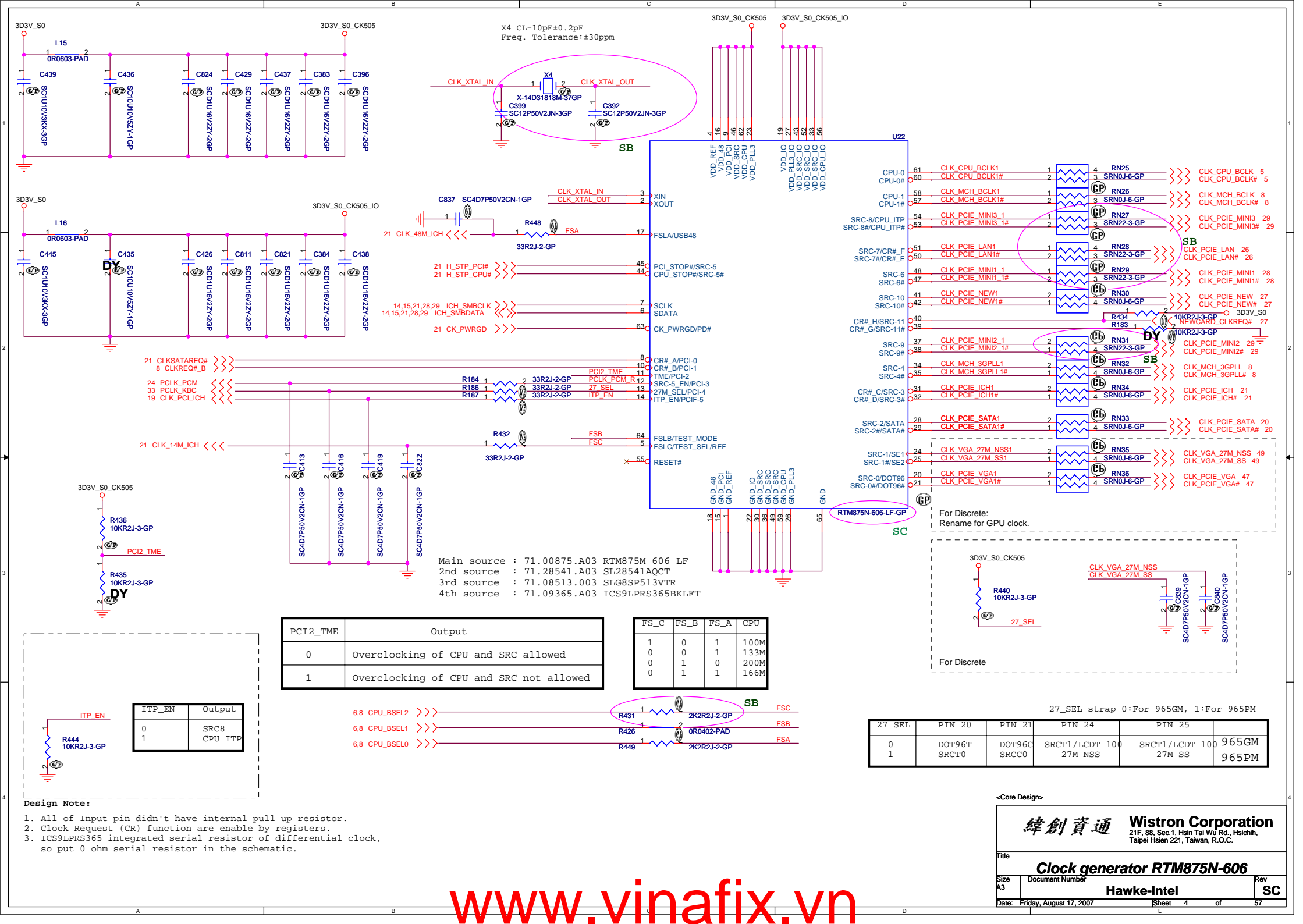
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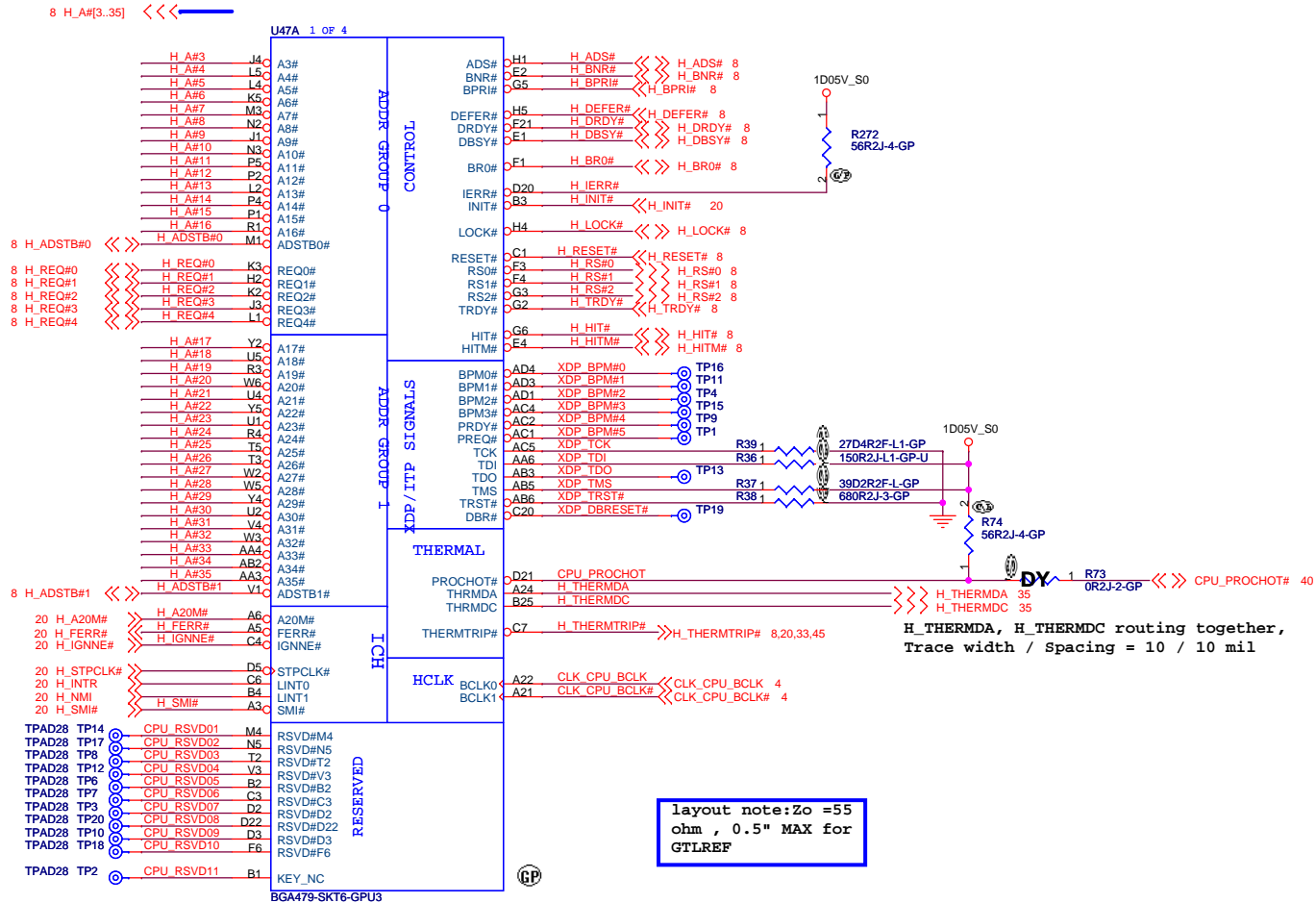
Title			Table of Content	
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## INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation





Main source : 62.10079.021 Tyco 2-1871873-4  
2nd source : 62.10040.221 Foxconn PZ47827-274M-41

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Title Meron(1/3)-AGTL+/XDP  
Size A3 Document Number Hawke-Intel Rev SC  
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8 H\_D#0[0.63] <<>>

8 H\_DSTBN#0  
8 H\_DSTBP#0  
8 H\_DINV#0

8 H\_DSTBN#1  
8 H\_DSTBP#1  
8 H\_DINV#1

4.8 CPU\_BSEL0  
4.8 CPU\_BSEL1  
4.8 CPU\_BSEL2

PLACE C617 close to the TEST4 PIN,  
make sure TEST3,TEST4,TEST5 trace  
routing is reference to GND and  
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

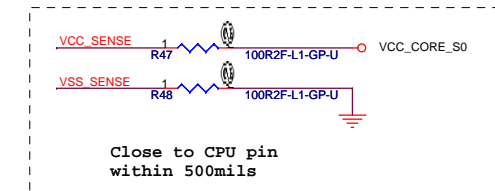
Resistor Placed  
within 0.5" of CPU  
pin. Trace should  
be at least 25 mils  
away from any other  
toggling signal .  
COMP[0,2] trace  
width is 18 mils.  
COMP[1,3] trace  
width is 4 mils .

VCC\_CORE\_S0

VCC\_CORE\_S0

layout note:  
place C618 near  
PIN B26

Length match within  
25 mils . The trace  
width/space/other is  
20/7/25 .



<Core Design>

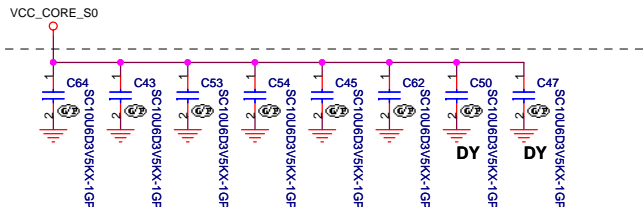
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Title			
Meron(2/3)-AGTL+-PWR			
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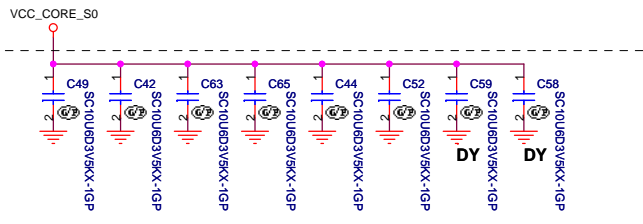
U47D 4 OF 4		
A4	VSS	P6
A8	VSS	P21
A11	VSS	P24
A14	VSS	R2
A16	VSS	R5
A19	VSS	R22
A23	VSS	R25
AF2	VSS	T1
B6	VSS	T4
B8	VSS	T23
B11	VSS	T26
B13	VSS	U3
B16	VSS	U6
B19	VSS	U21
B21	VSS	U24
B24	VSS	V2
C5	VSS	V5
C8	VSS	V22
C11	VSS	V25
C14	VSS	W1
C16	VSS	W4
C19	VSS	W23
C2	VSS	W26
C22	VSS	Y3
C25	VSS	Y6
D1	VSS	Y21
D4	VSS	Y24
D8	VSS	AA2
D11	VSS	AA5
D13	VSS	AA8
D16	VSS	AA11
D19	VSS	AA14
D23	VSS	AA16
D26	VSS	AA19
E3	VSS	AA22
E6	VSS	AA25
E8	VSS	AB1
E11	VSS	AB4
E14	VSS	AB8
E16	VSS	AB11
E19	VSS	AB13
E21	VSS	AB16
E24	VSS	AB19
F5	VSS	AB23
F8	VSS	AB26
F11	VSS	AC3
F13	VSS	AC6
F16	VSS	AC8
F19	VSS	AC11
F2	VSS	AC14
F22	VSS	AC16
F25	VSS	AC19
G4	VSS	AC21
G1	VSS	AC24
G23	VSS	AD2
G26	VSS	AD5
H3	VSS	AD8
H6	VSS	AD11
H21	VSS	AD13
H24	VSS	AD16
J2	VSS	AD19
J5	VSS	AD22
J22	VSS	AD25
J25	VSS	AE1
K1	VSS	AE4
K4	VSS	AE8
K23	VSS	AE11
K26	VSS	AE14
L3	VSS	AE16
L6	VSS	AE19
L21	VSS	AE23
L24	VSS	AE26
M2	VSS	A2
M5	VSS	AF6
M22	VSS	AF8
M25	VSS	AF11
N1	VSS	AF13
N4	VSS	AF16
N23	VSS	AF19
N26	VSS	AF21
P3	VSS	A25
	VSS	AF25

BGA479-SKT6-GPU3

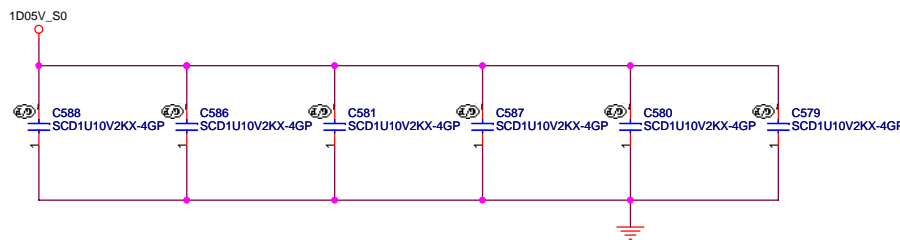
Place these capacitors on L1  
(North side ,Secondary Layer)



Place these capacitors on L1  
(North side ,Secondary Layer)



Mid Frequencd  
Decoupling

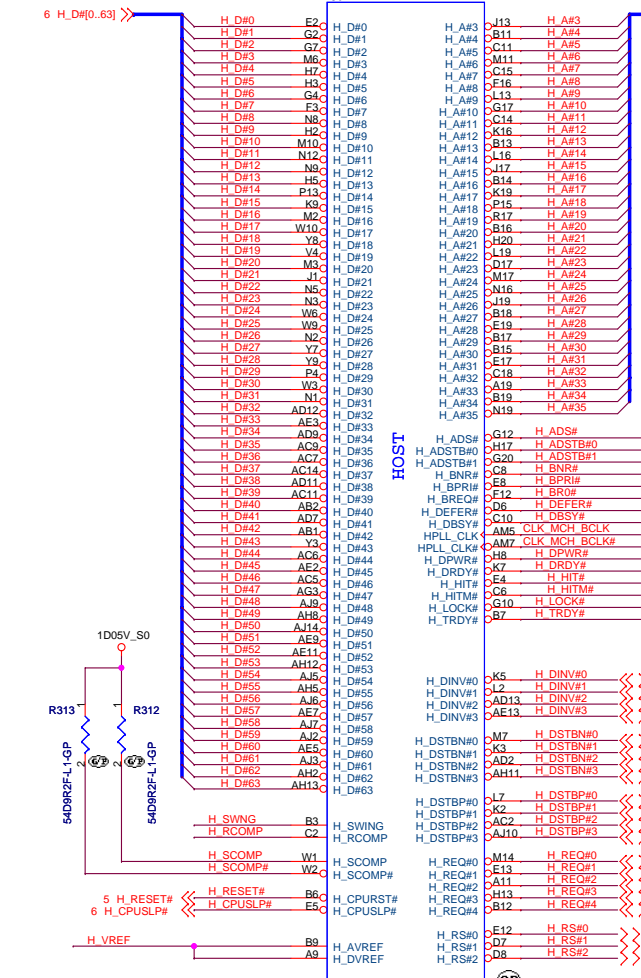


Place these  
inside socket  
cavity on L1  
(North side  
Secondary)

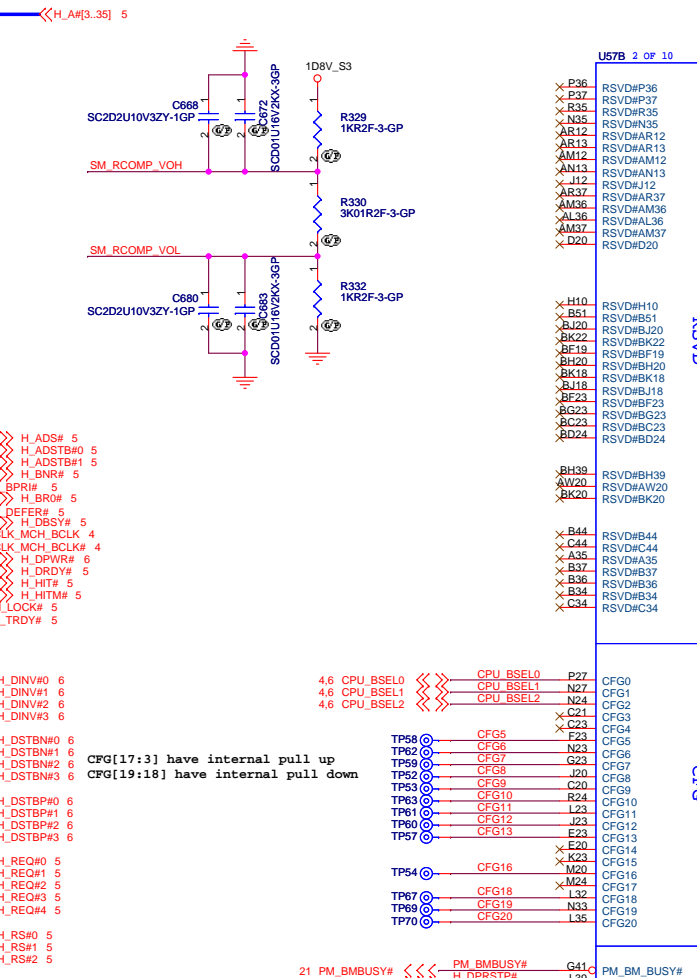
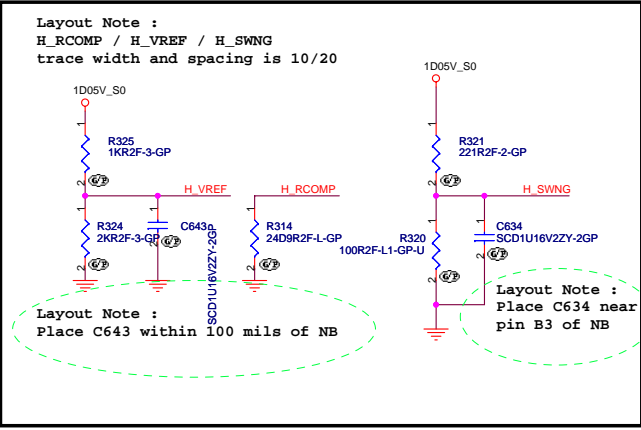
<Core Design>

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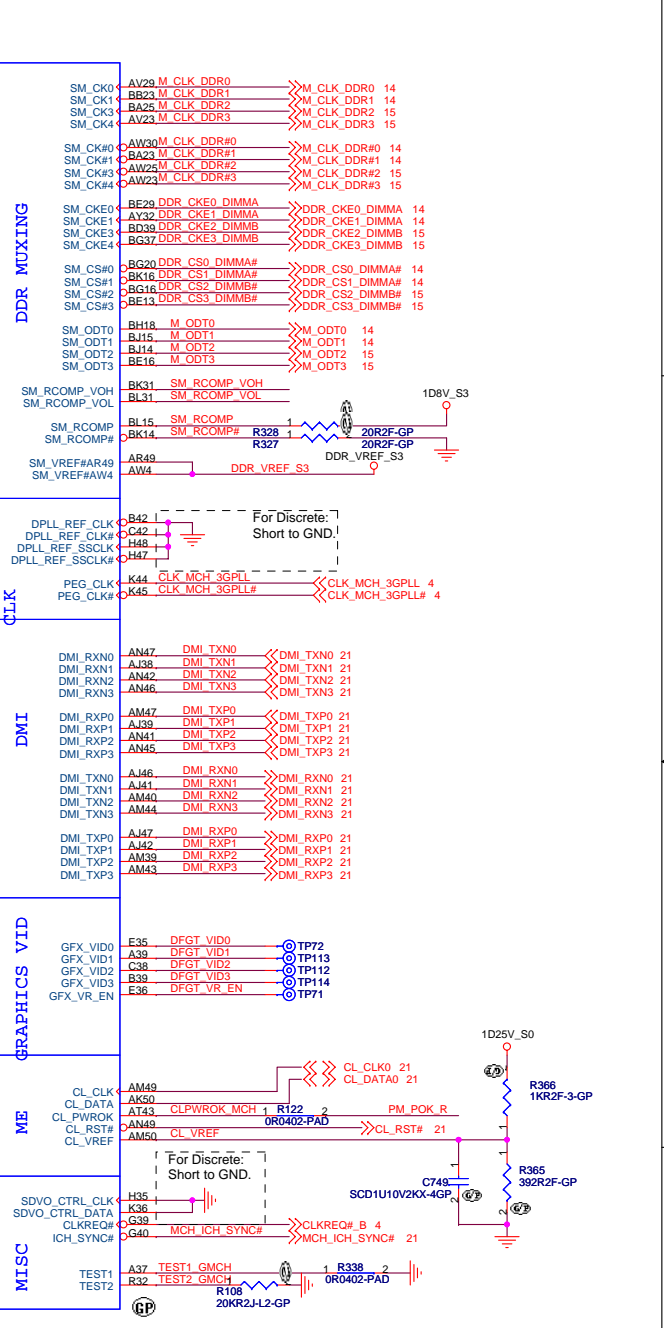
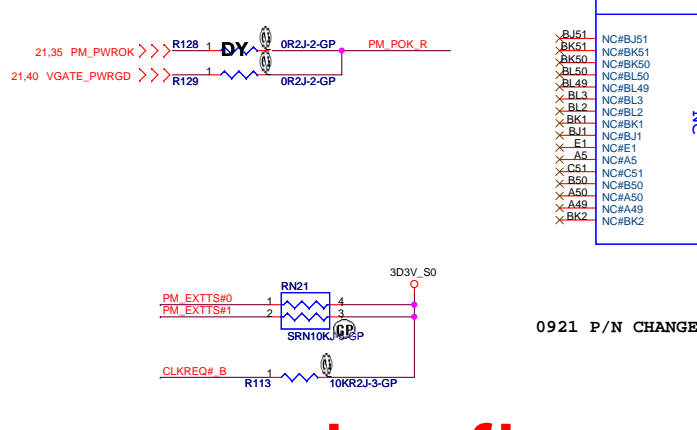
Title		
Meron(3/3)-GND&Bypass		
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layout note :  
Route H\_SCOMP# and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



layout note :  
Route H\_SCOMP# and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



0921 P/N CHANGE TO 71.CREST.M02

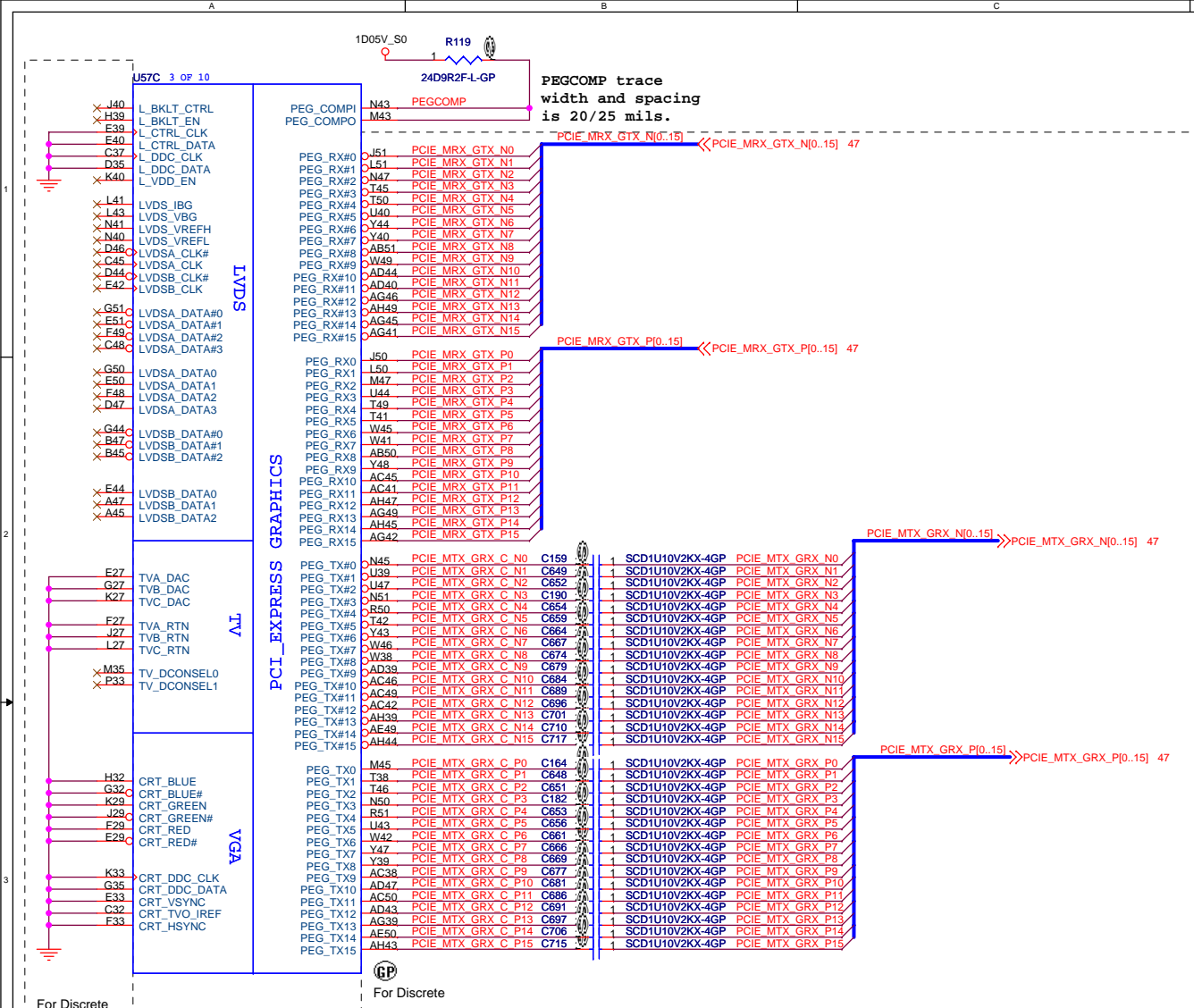
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CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size Custom Document Number Hawke-Intel Rev SC

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## Strap Pin Table

CFG[2:0] FSB Freq select

CFG5 (DMI select)

CFG6

CFG7 (CPU Strap)

CFG8 (Low power PCIE)

CFG9 (PCIE Graphics Lane Reversal)

CFG[11:10]

CFG[13:12] (XOR/ALLZ)

CFG[15:14]

CFG16 (FSB Dynamic ODT)

CFG[18:17]

SDVO\_CTRLDATA

CFG19(DMI Lane Reversal)

CFG20(PCIE/SDVO consurrent)

010 = FSB 800MHz  
011 = FSB 667MHz  
Others = Reserved

0 = DMI x 2  
1 = DMI x 4 \*

Reserved

0 = Reserved  
1 = Mobile CPU \*

0 = Normal mode  
1 = Low Power mode \*

0 = Reverse Lane  
1 = Normal Operation \*

Reserved

00 = Reserved  
01 = XOR Mode Enabled  
10 = All Z Mode Enabled  
11 = Normal Operation (Default)\*

Reserved

0 = Disable  
1 = Enable \*

Reversed

0 = No SDVO Device Present \*  
1 = SDVO Device Present

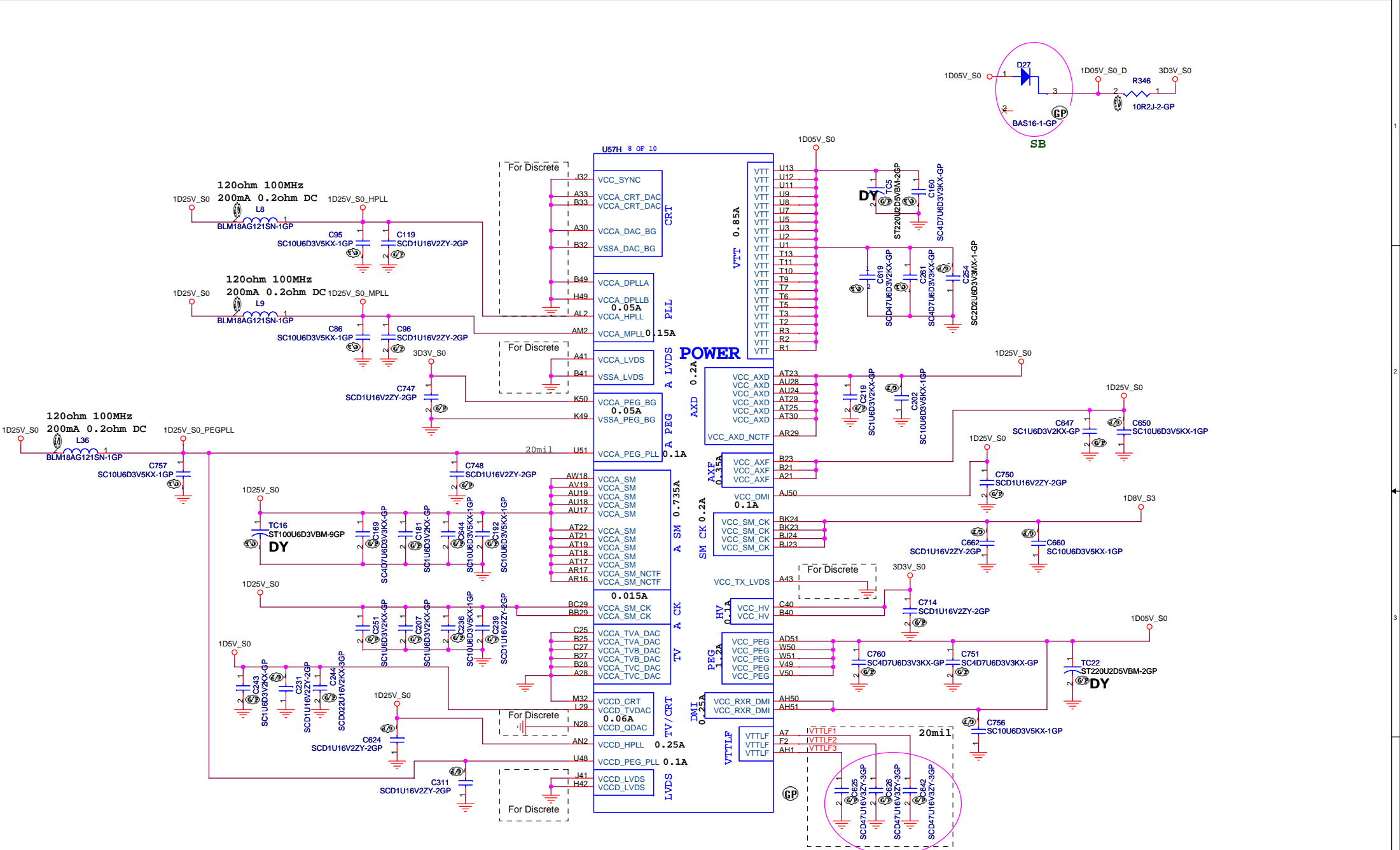
0 = Normal Operation  
(Lane number in Order)  
1 = Reverse lane \*

0 = Only PCIE or SDVO is operational \*  
1 = PCIE/SDVO are operating simu.

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Title		CRESTLINE(3/6)-VGA/LVDS/TV	
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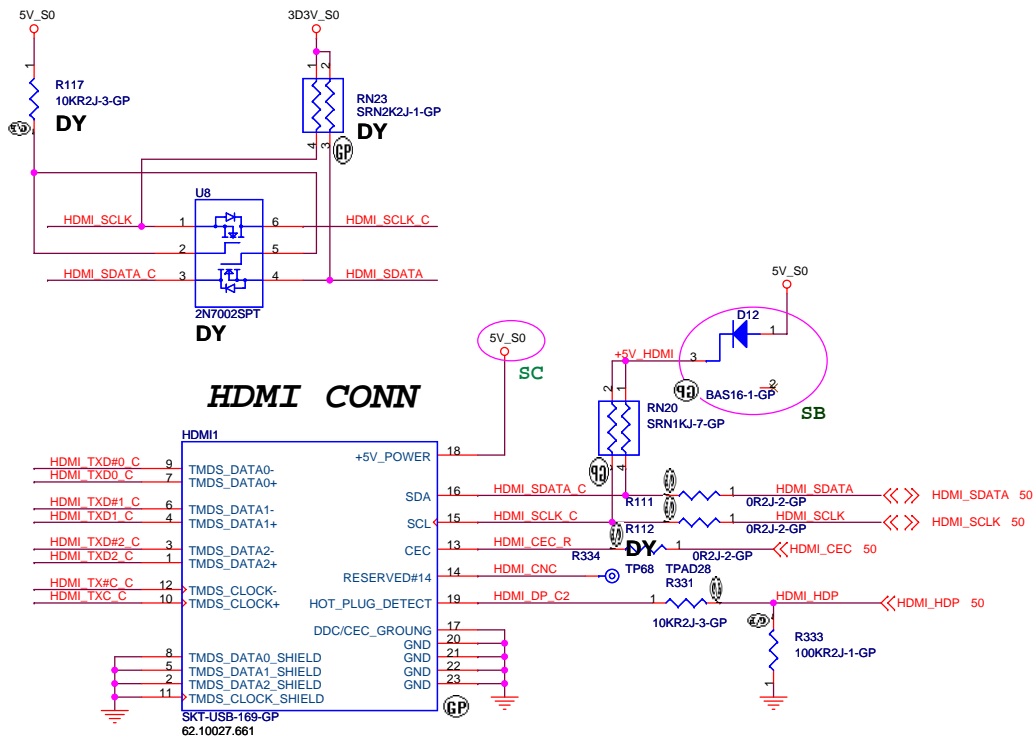
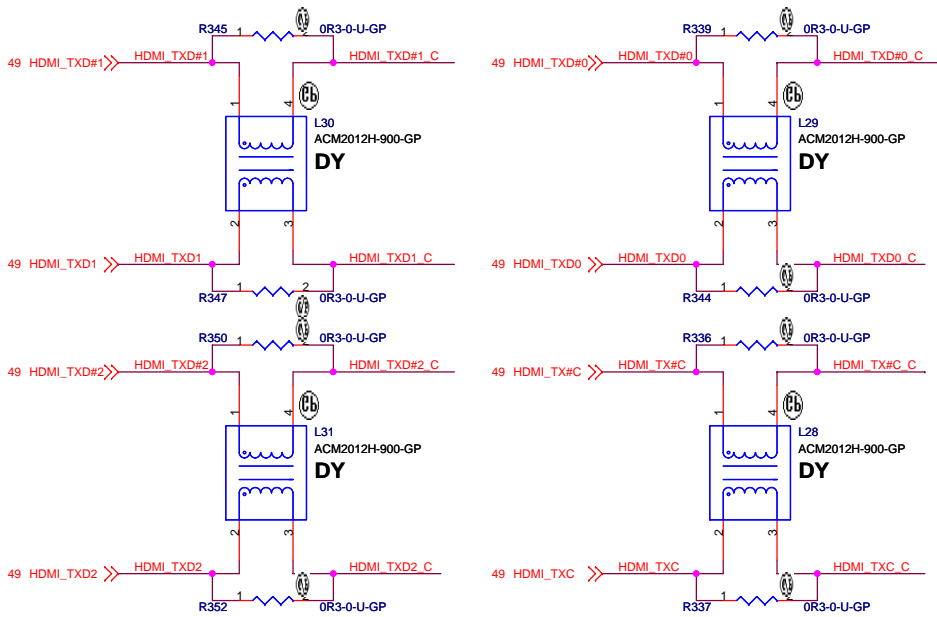






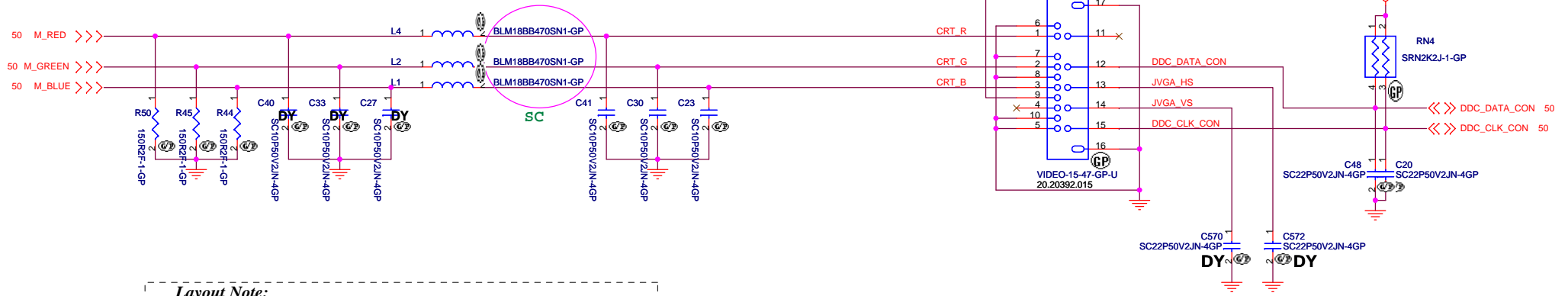


HDMI I/F & CONNECTOR



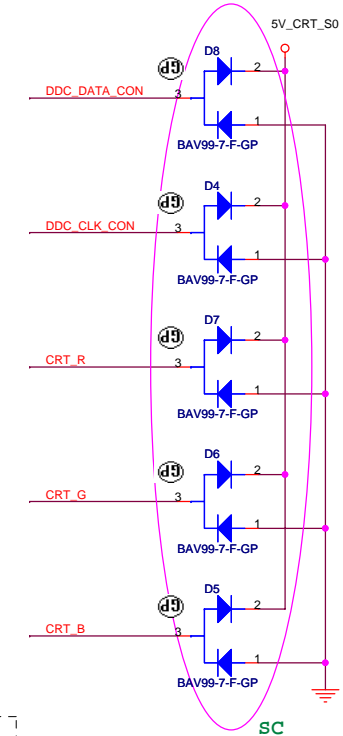
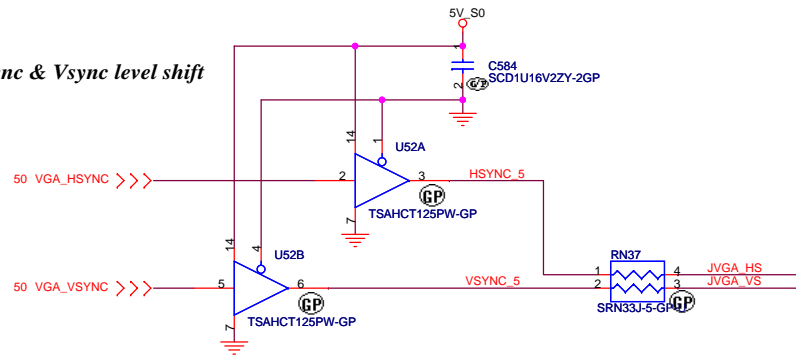
Main source : 62.10027.661 Molex 47408-0201  
2nd source : 62.10078.121 Tyco C1759548-1

# CRT I/F & CONNECTOR



**Layout Note:**  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## Hsync & Vsync level shift



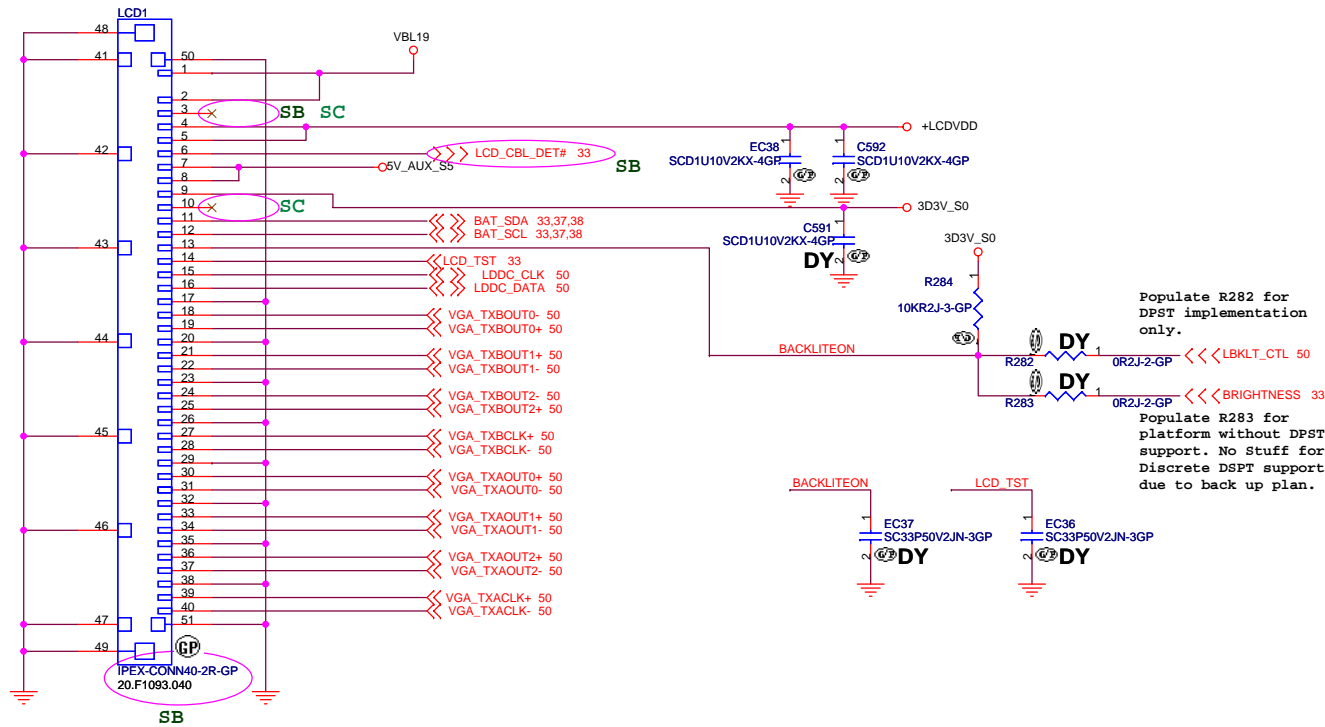
TP28-75-GP	TP177	1	5V_CRT_S0
TP28-75-GP	TP176	1	DDC_DATA_CON
TP28-75-GP	TP179	1	DDC_CLK_CON
TP28-75-GP	TP178	1	CRT_R
TP28-75-GP	TP180	1	CRT_G
TP28-75-GP	TP182	1	CRT_B
TP28-75-GP	TP181	1	JVGA_HS
TP28-75-GP	TP183	1	JVGA_VS

For AFTE, place them on the same side.

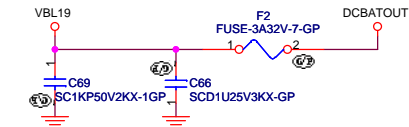
<Core Design>

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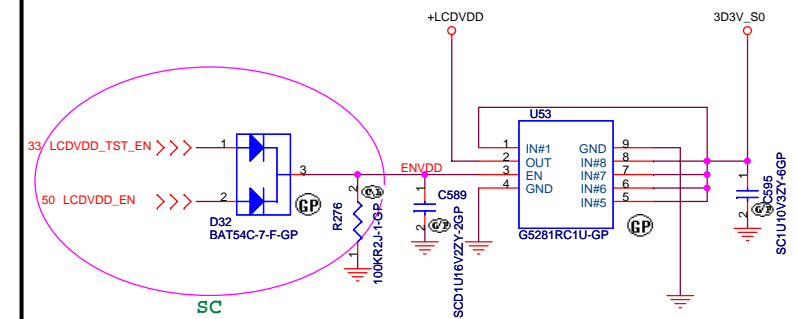
Title	<b>CRT Connector</b>	
Size A3	Document Number	Rev
	<b>Hawke-Intel</b>	<b>SC</b>
Date: Friday, August 17, 2007	Sheet 17	of 57



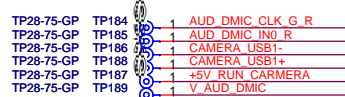
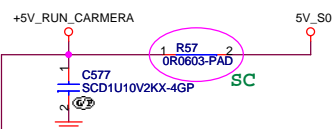
## INVERTER POWER



## LCD POWER

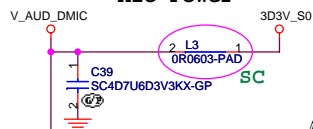


## CAMERA Power

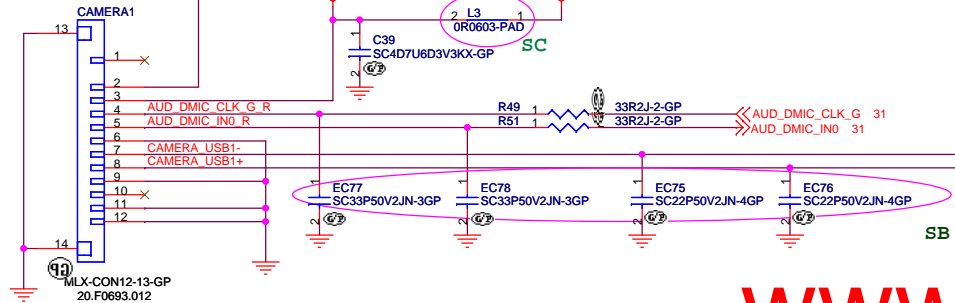
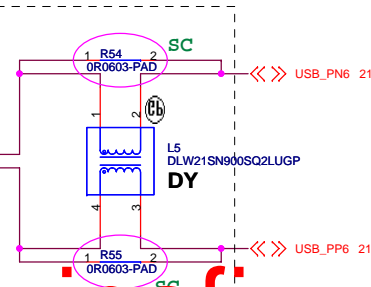


For AFTE, place them on the some side.

## Mic Power



Place near connector CAMERA1.



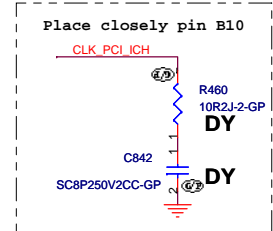
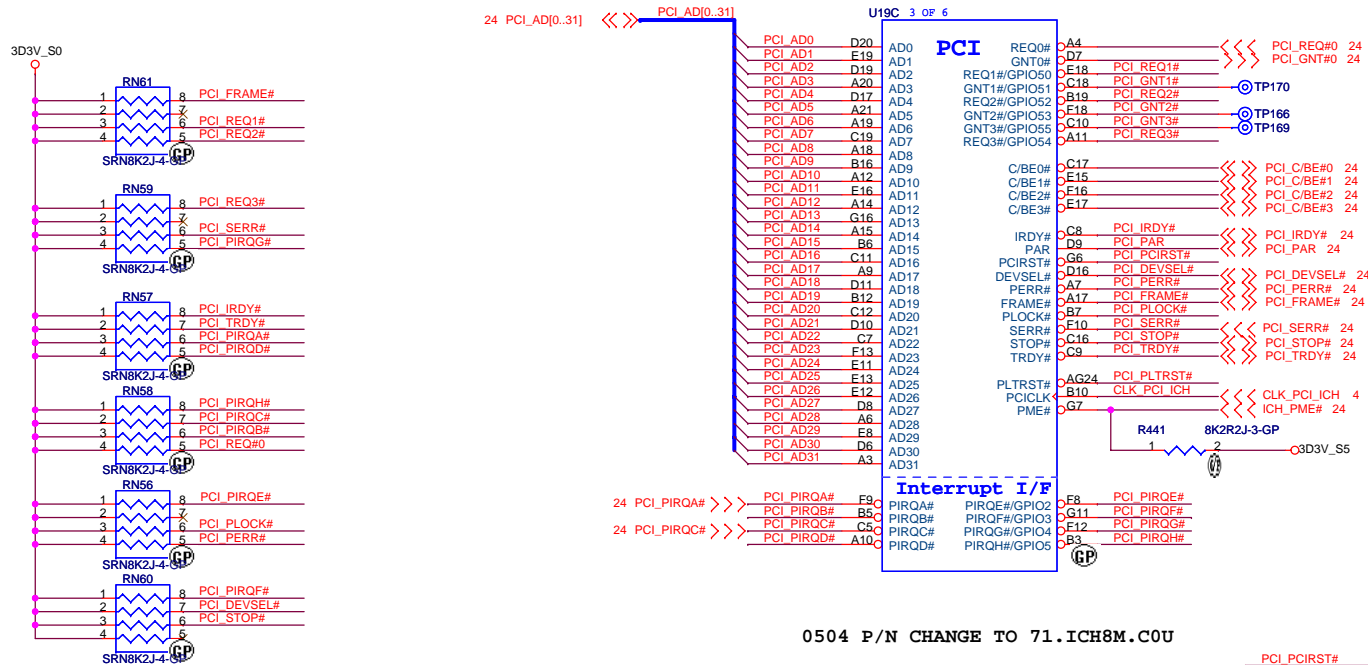
<Core Design>

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Title				
LCD/Inverter/Camera				
Size A3	Document Number			Rev
	Hawke-Intel			SC
Date:	Friday, August 17, 2007	Sheet	18	of 57

# PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

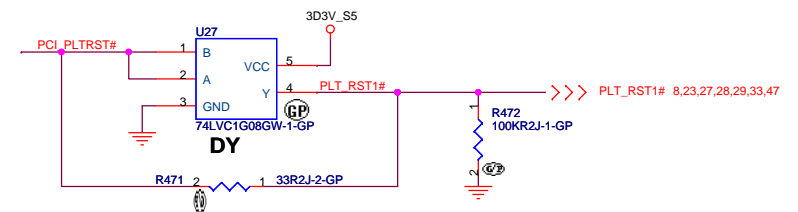
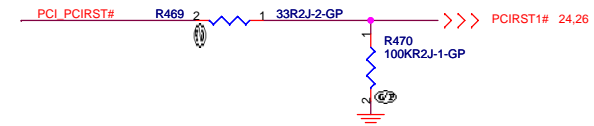
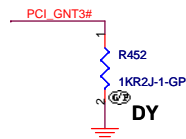


0504 P/N CHANGE TO 71.ICH8M.C0U

## ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

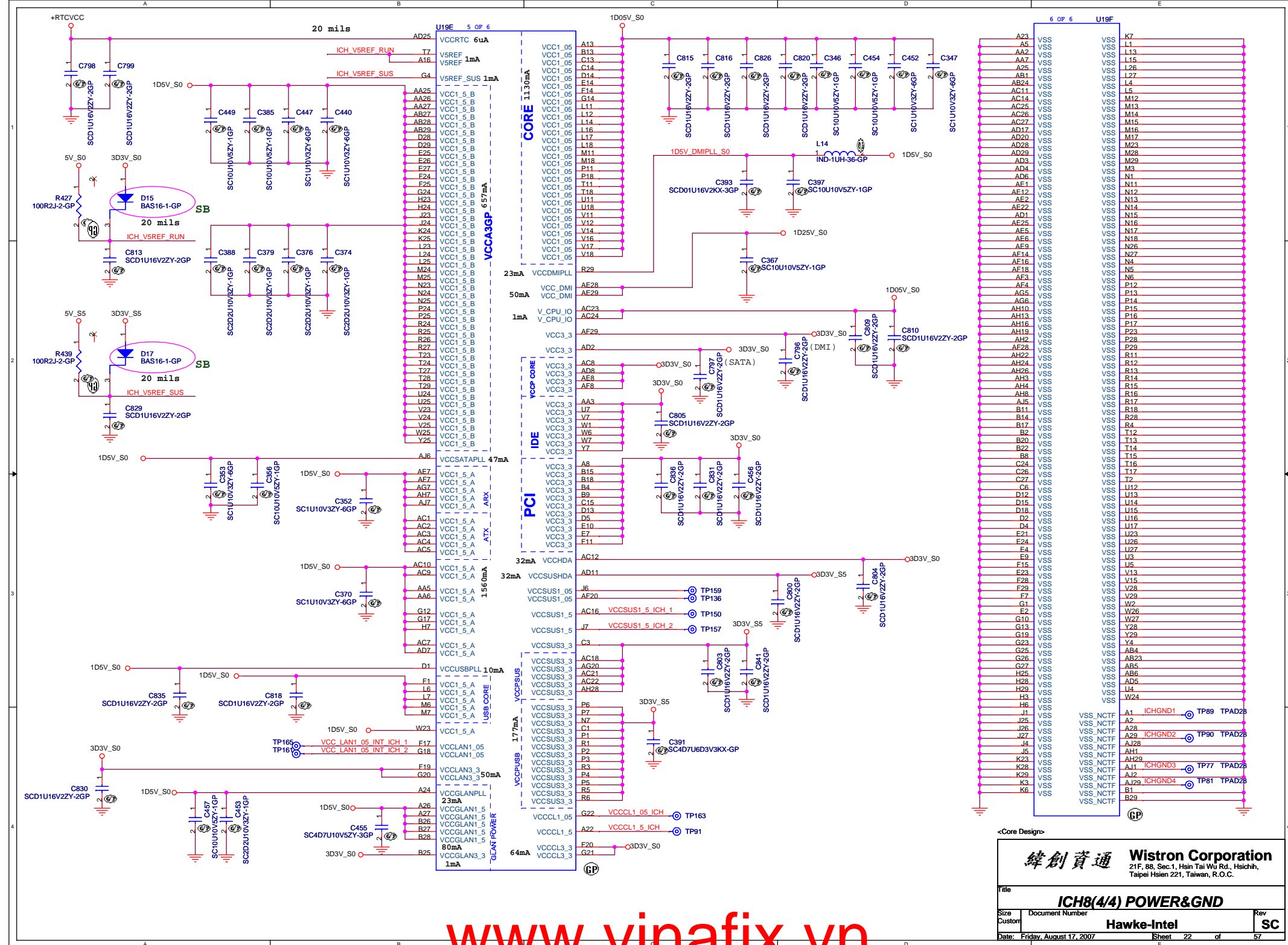


<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH8(1/4)-PCI/INT
Size A3	Document Number
Date: Friday, August 17, 2007	Sheet 19 of 57
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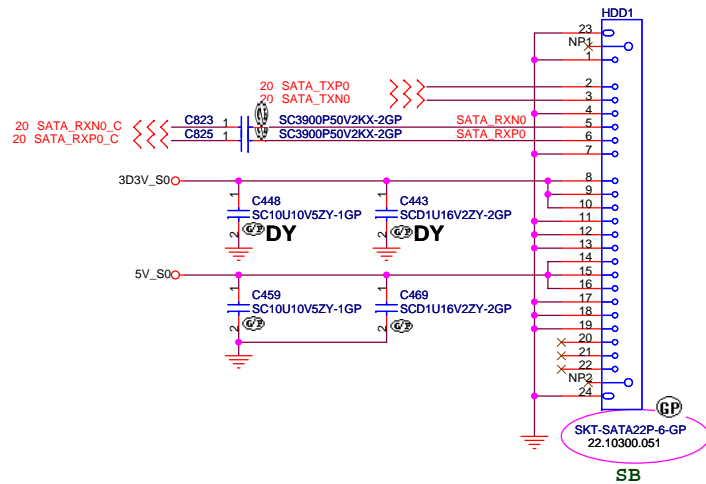
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File: **ICH8(4/4) POWER&GND**

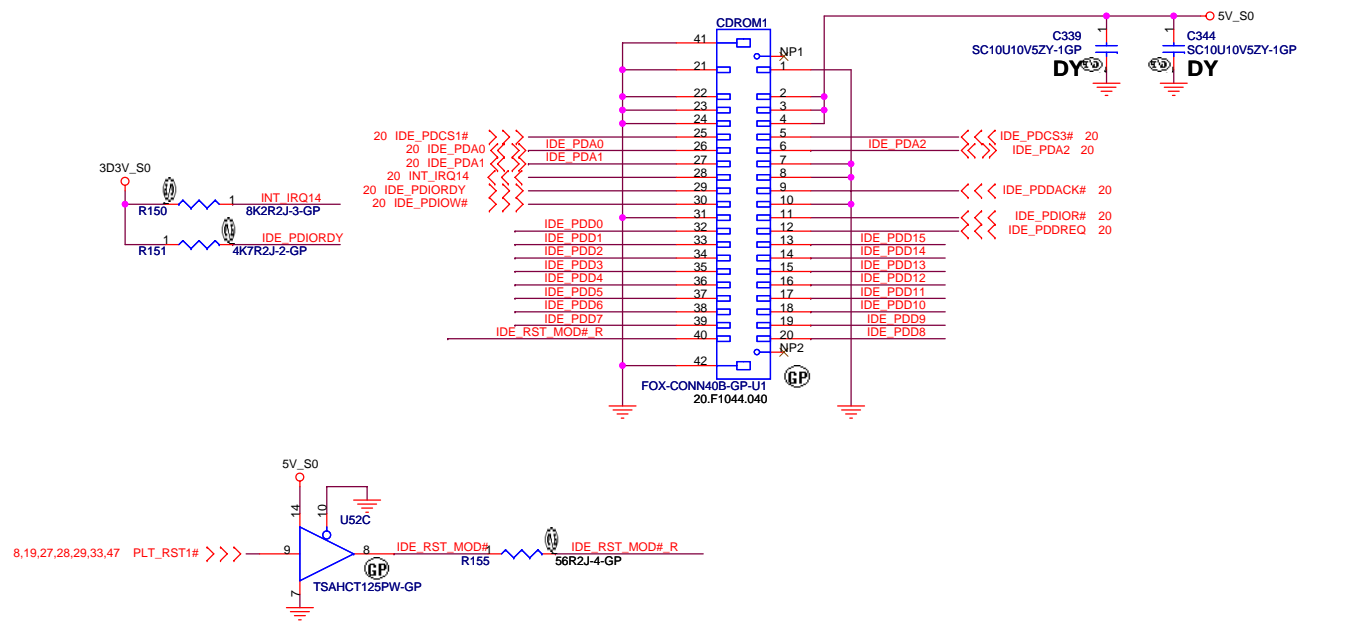
Size	Document Number	Rev
Custom	<b>Hawke-Intel</b>	<b>SC</b>
Date: Friday, August 17, 2007	Sheet 22 of 57	

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# SATA HDD Connector



# ODD Connector



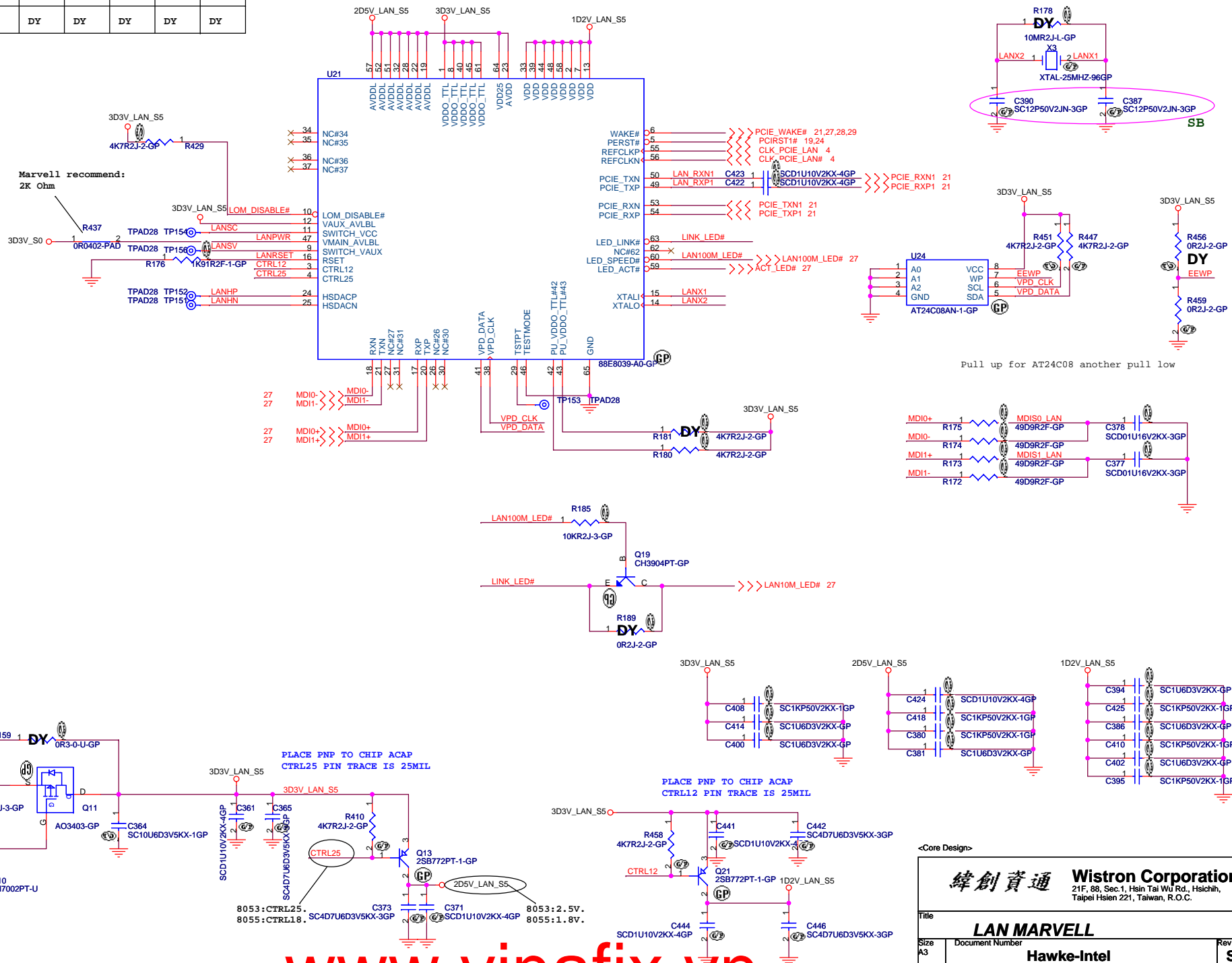
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		<b>HDD/ODD</b>	
Size A3	Document Number	<b>Hawke-Intel</b>	Rev <b>SC</b>
Date: Friday, August 17, 2007		Sheet 23 of	57



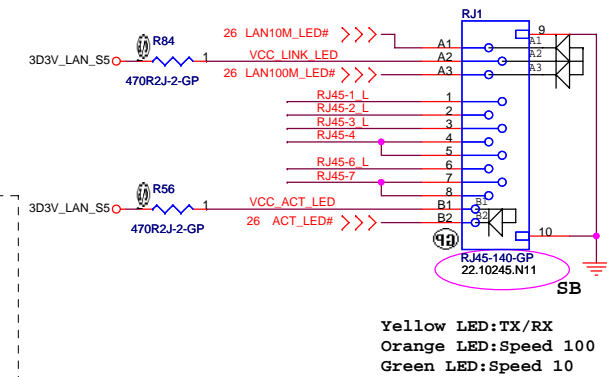
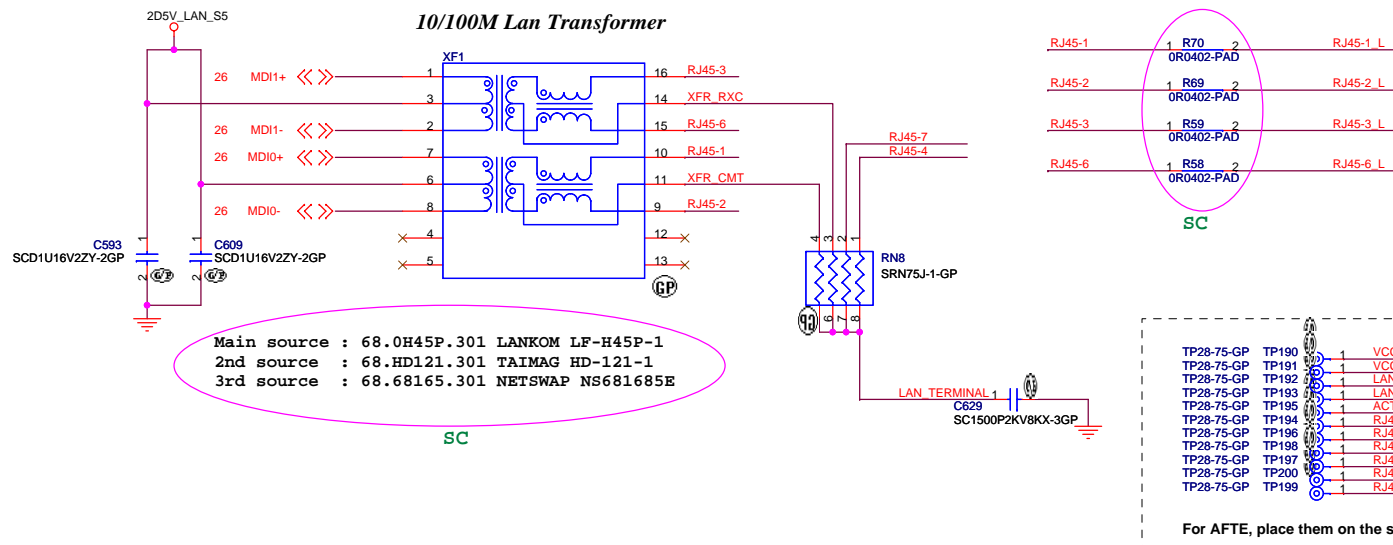


	R181	R176	R172	R173	R174	R175	C377	C378
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY



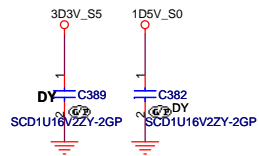
# RJ45 Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

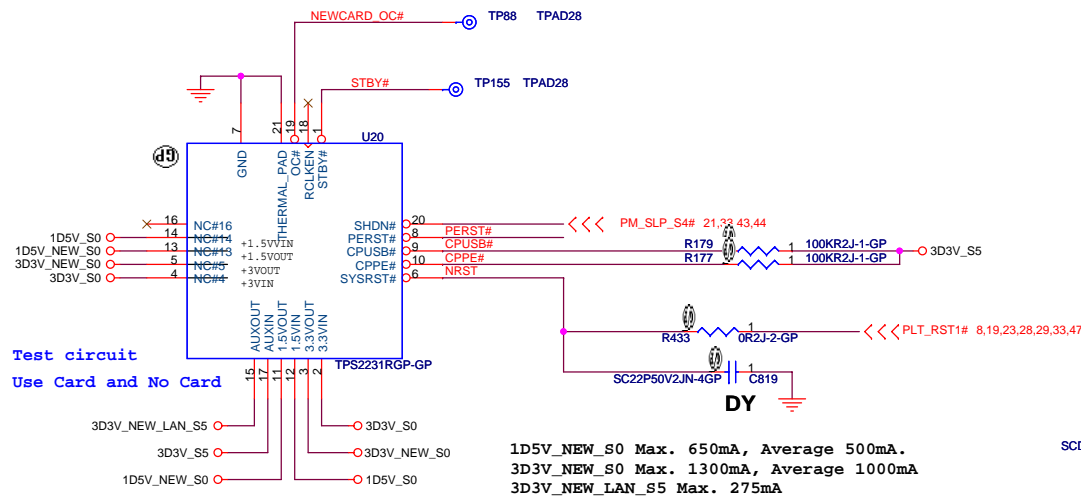
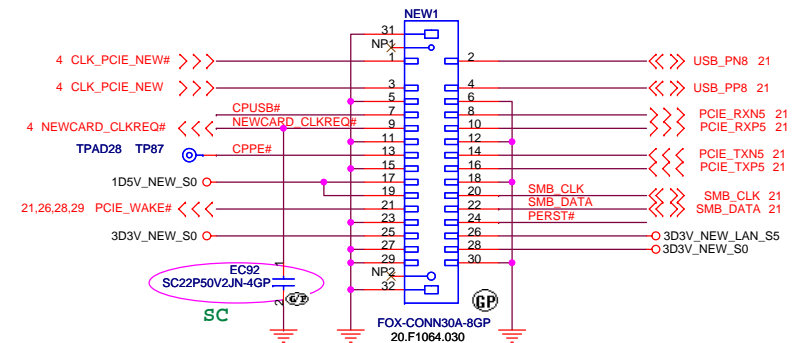
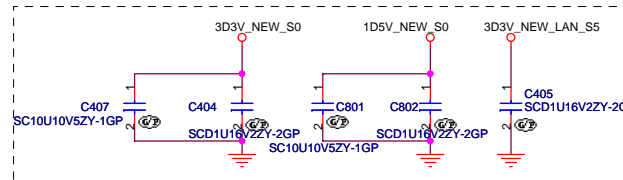


# NEWCARD Connector

Place them Near to Chip



Place them Near to Connector

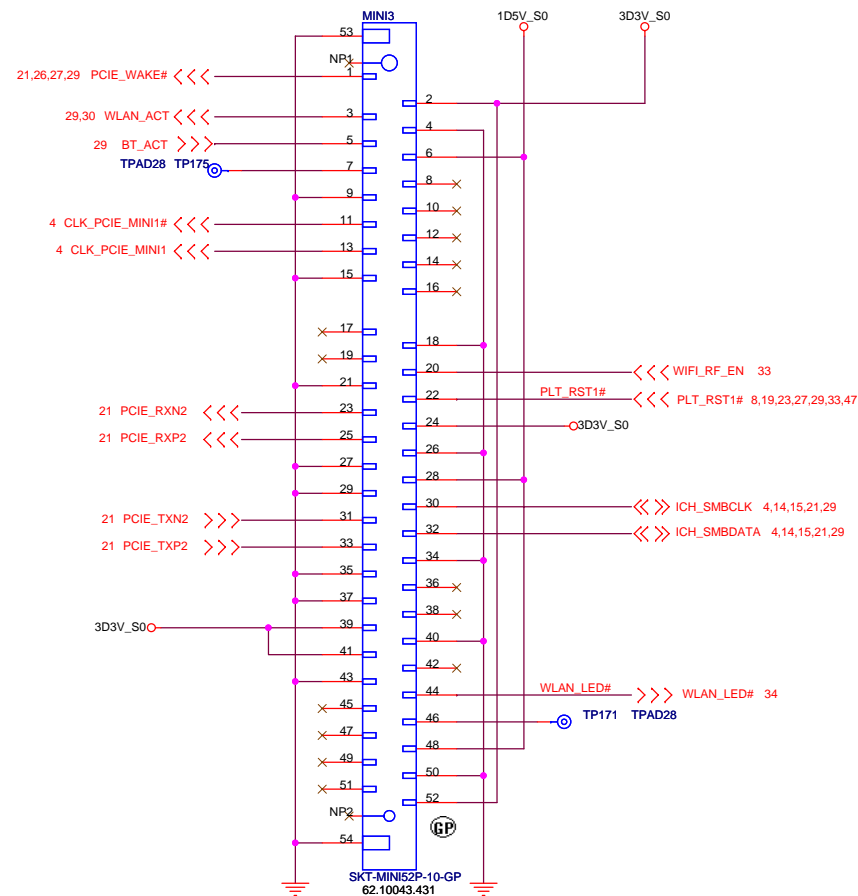


<Core Design>

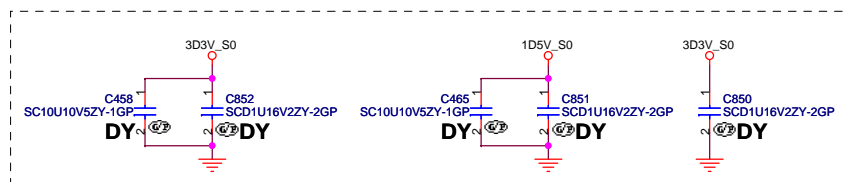
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>LAN connector/NEW CARD</b>		
Size	Document Number	Rev
A3	<b>Hawke-Intel</b>	<b>SC</b>
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# Mini Card Connector 1(802.11a/b/g)



Main source : 20.F0992.052 P-Two A54452-A0G16-N  
2nd source : 62.10043.551 Tyco 1759553-1

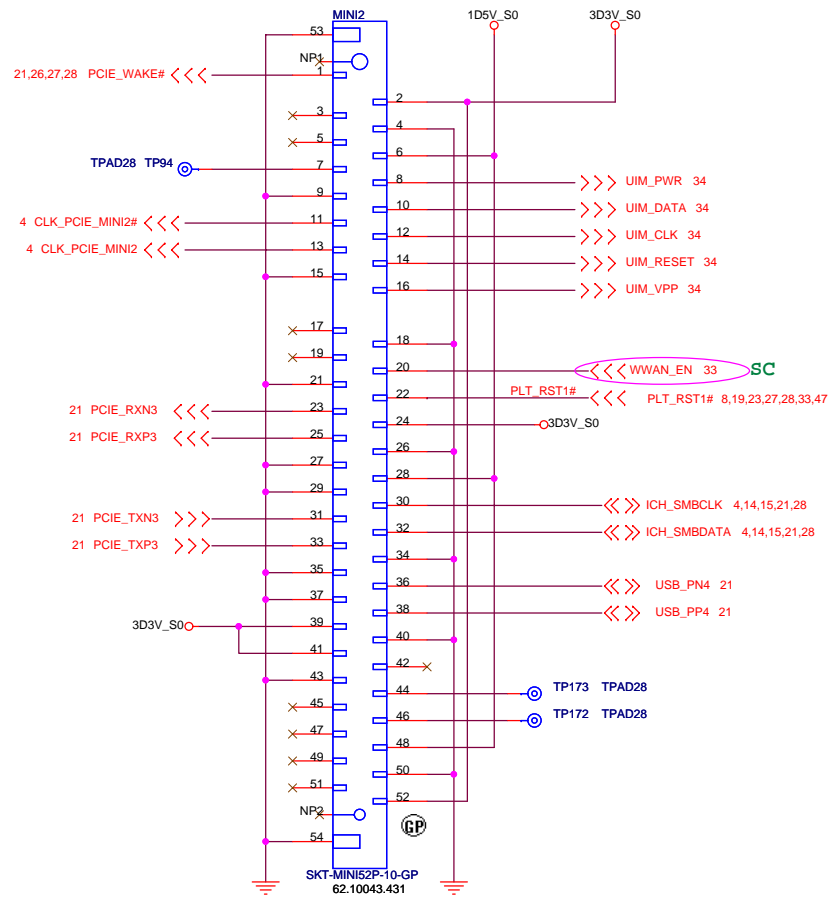


<Core Design>

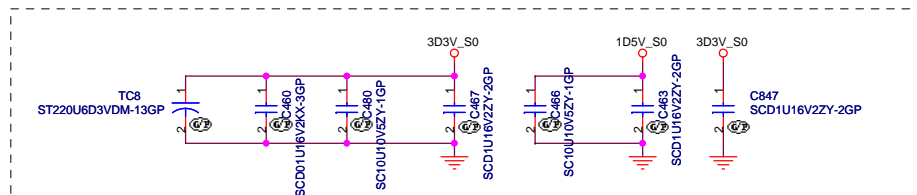
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MINI CARD CONN 1</b>	
Size A3	Document Number
<b>Hawke-Intel</b>	
Date: Friday, August 17, 2007	Sheet 28 of 57
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# Mini Card Connector

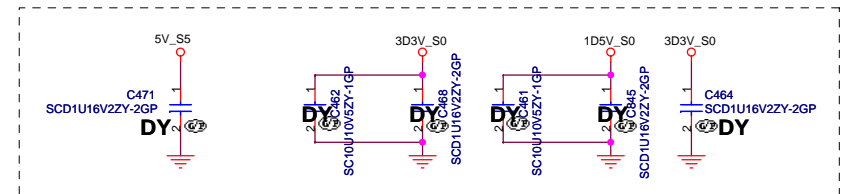
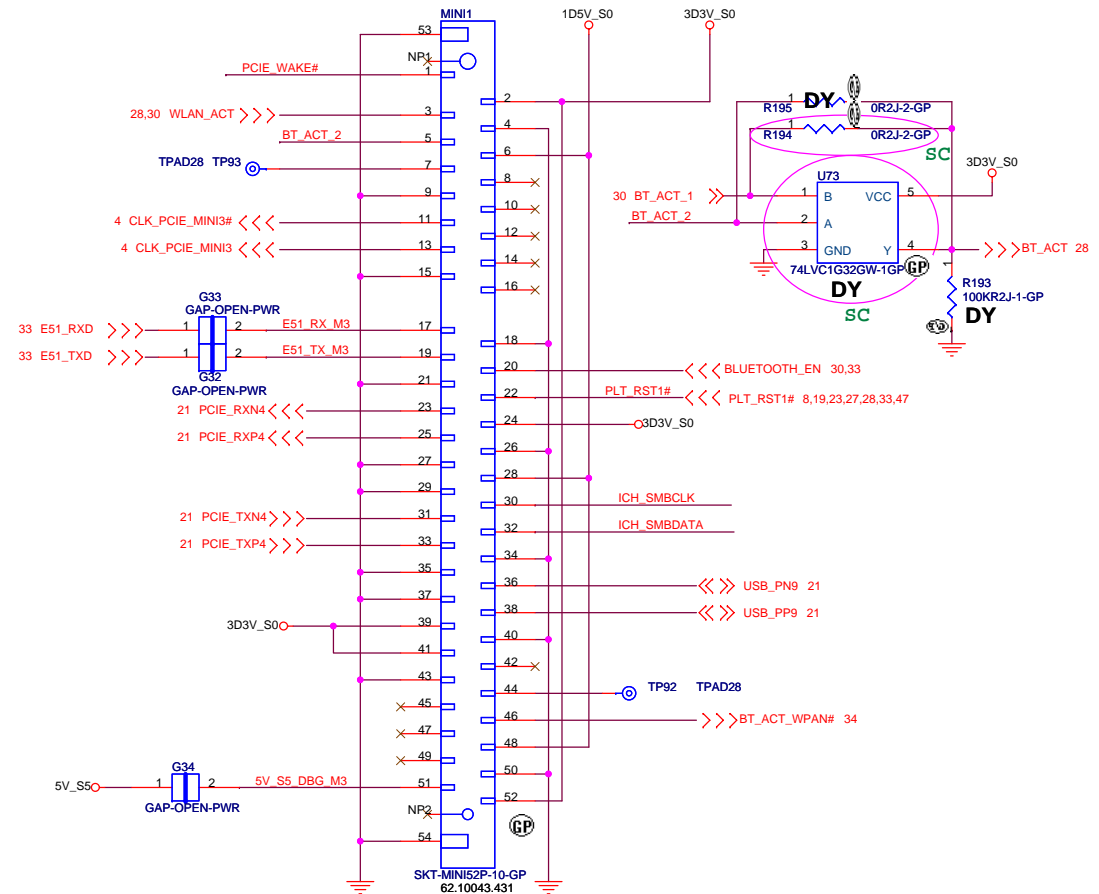
## Mini Card Connector 2(WWAN)



Main source : 20.F0992.052 P-Two A54452-A0G16-N  
2nd source : 62.10043.551 Tyco 1759553-1

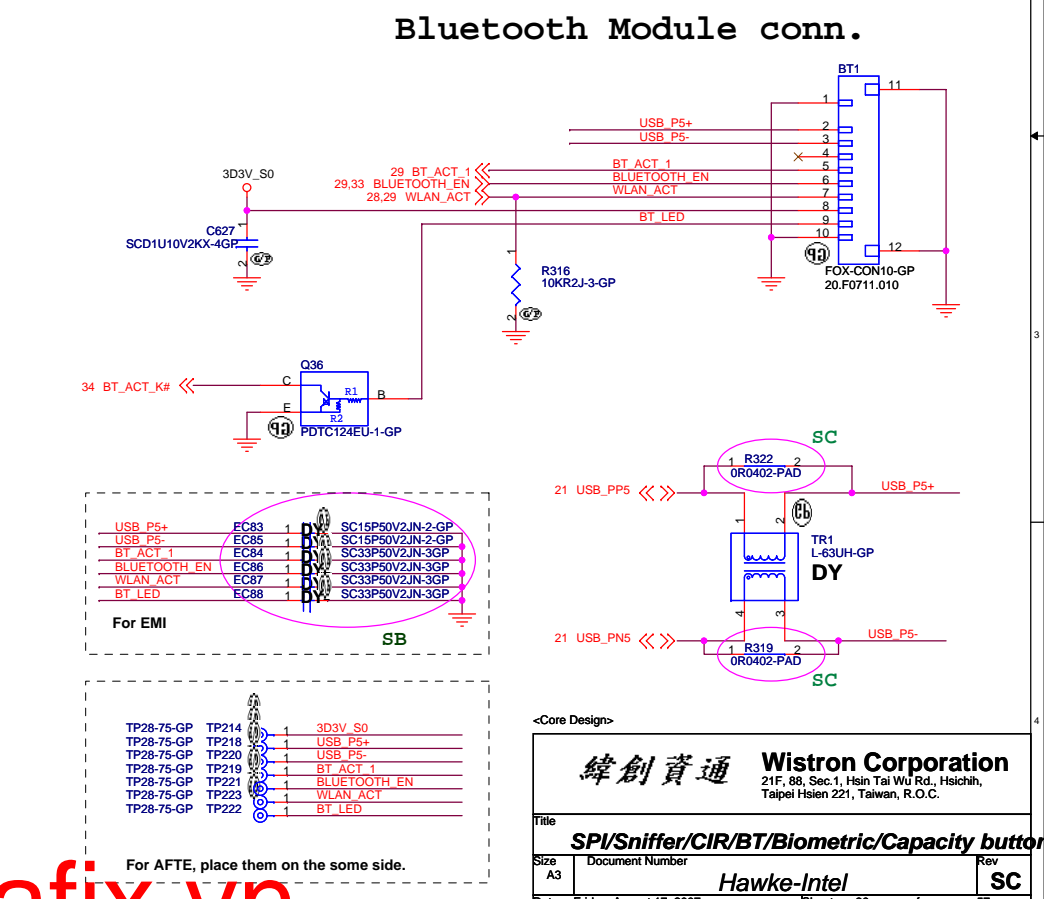
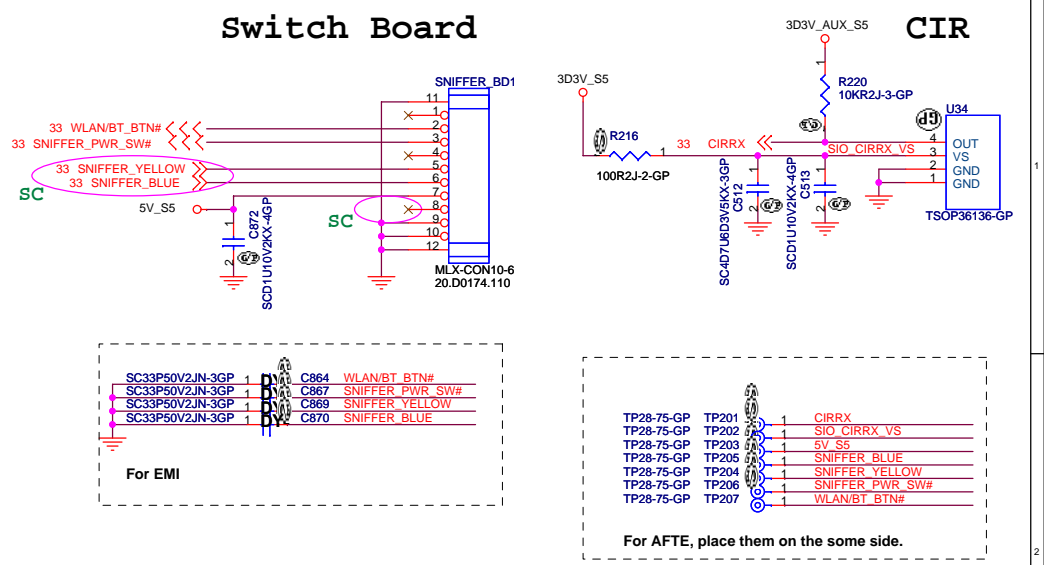
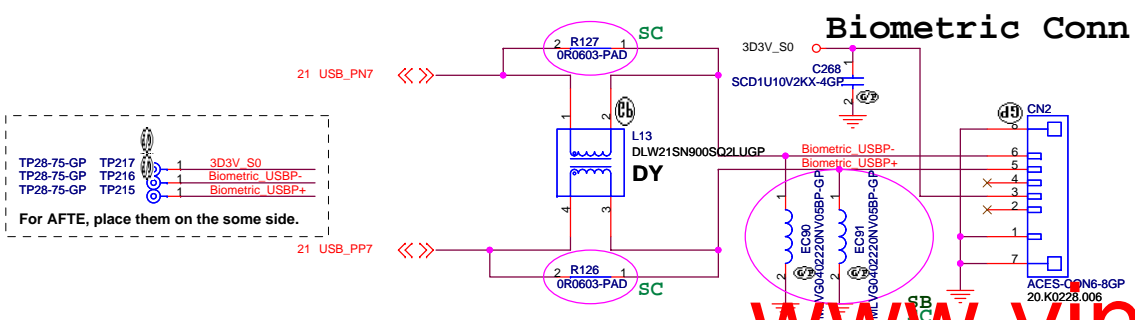
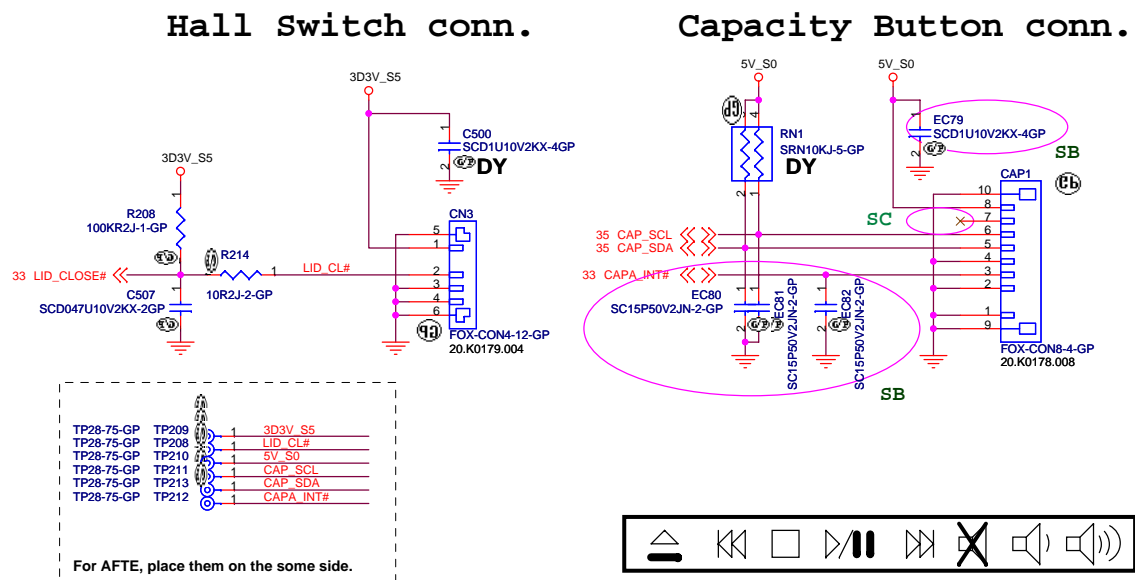
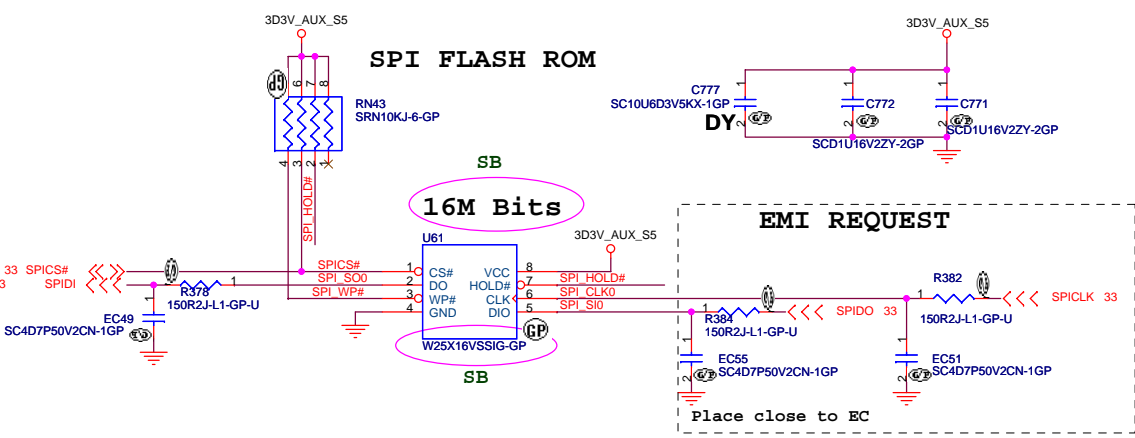


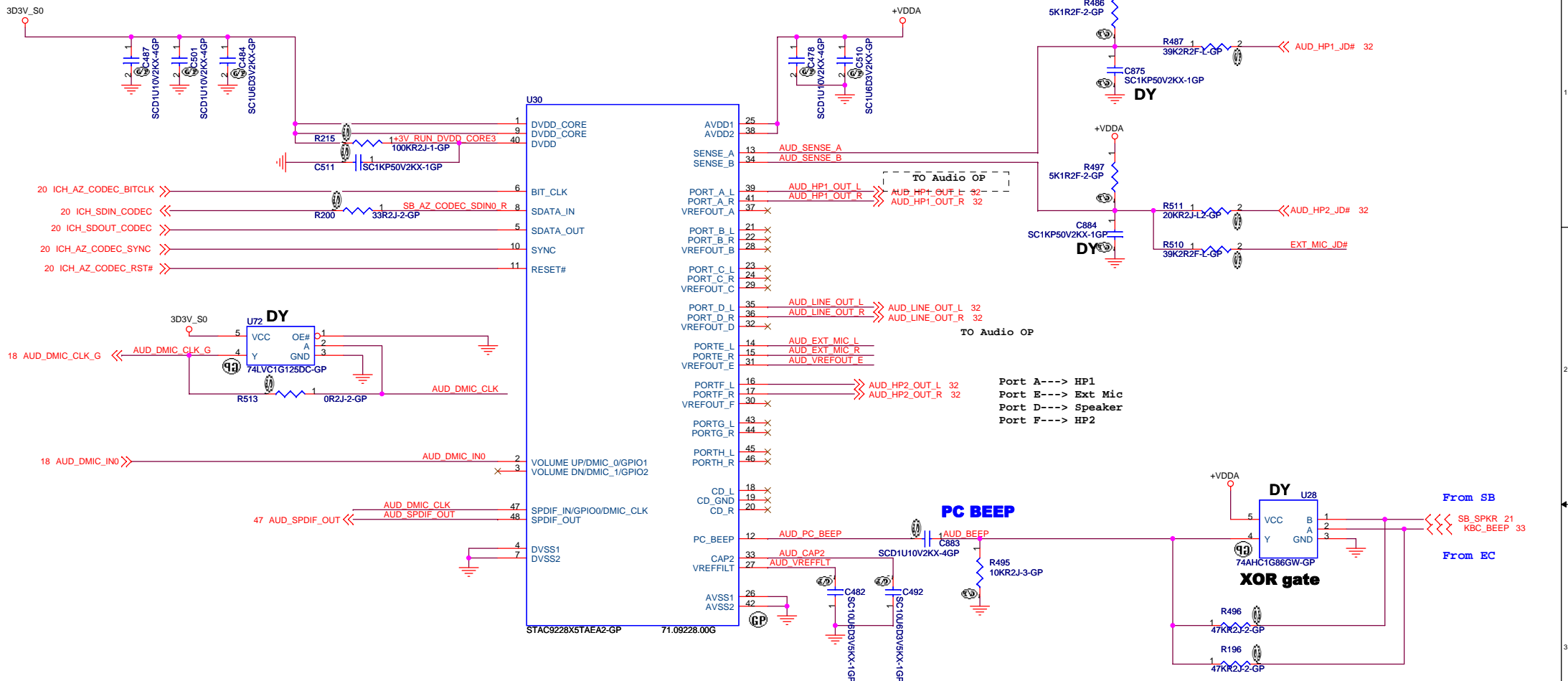
# Mini Card Connector 3(Robson/BT)



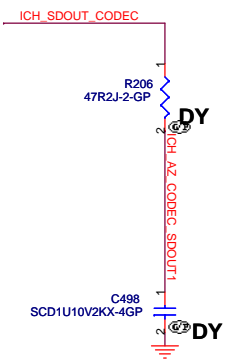
<Core Design>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Size		
A3		
Document Number		
Hawke-Intel		
Date: Friday, August 17, 2007		
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SC		

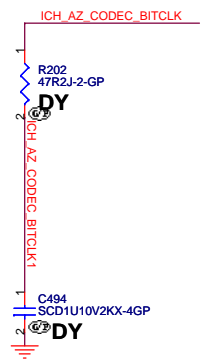




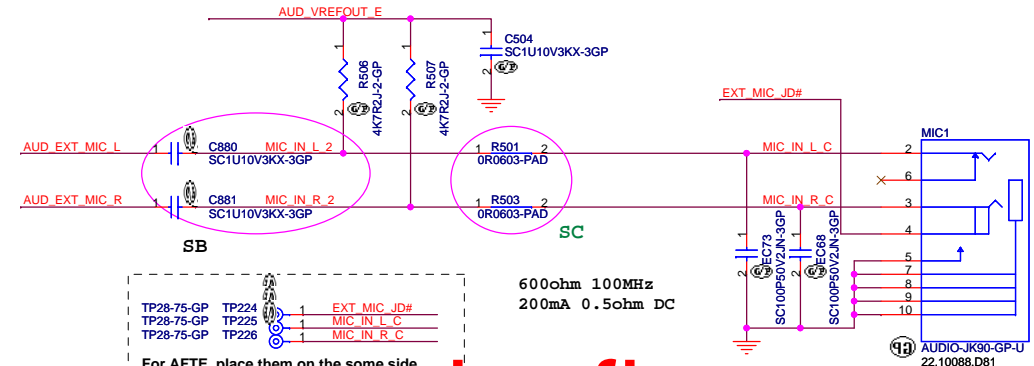
#### Azalia I/F EMI



#### Azalia I/F EMI



#### MIC IN



<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

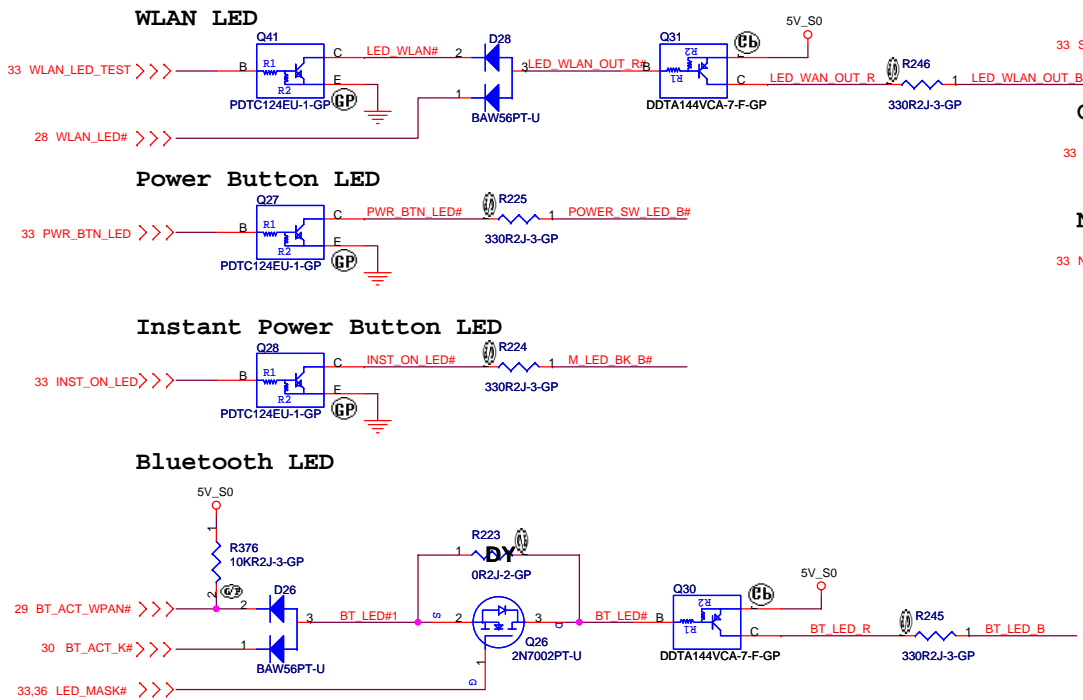
Title: **AUDIO CODEC STAC9228**

Size: A3	Document Number: <b>Hawke-Intel</b>	Rev: <b>SC</b>
Date: Friday, August 17, 2007	Sheet: 31 of 57	

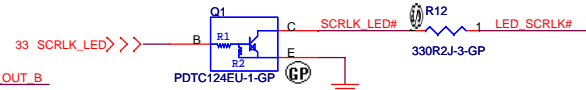
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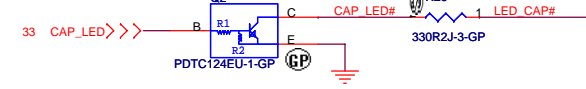




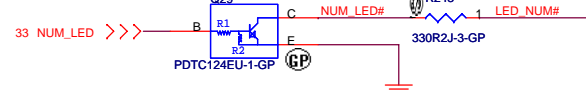
## SCRLK LED



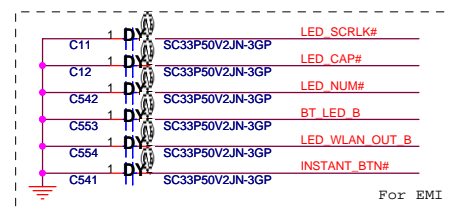
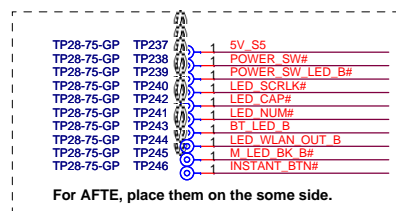
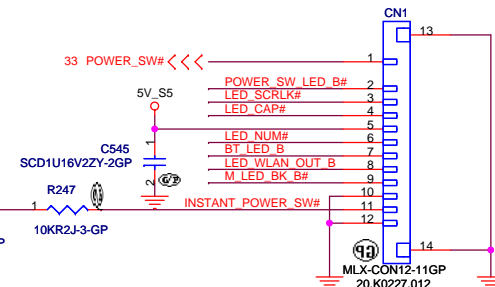
## CAPS LED



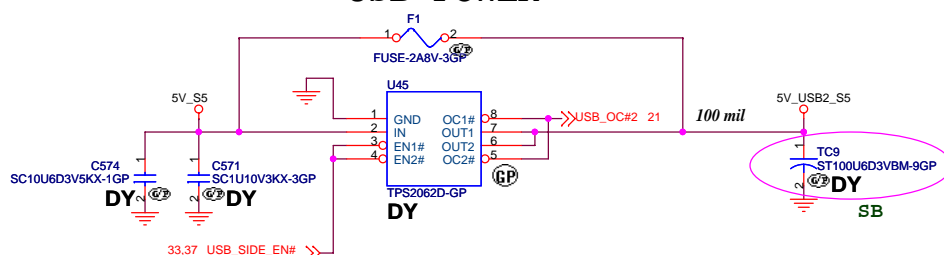
## NUM LED



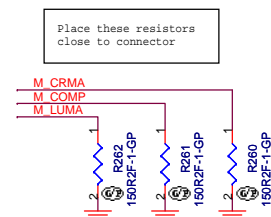
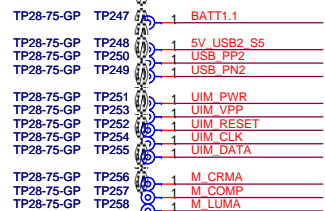
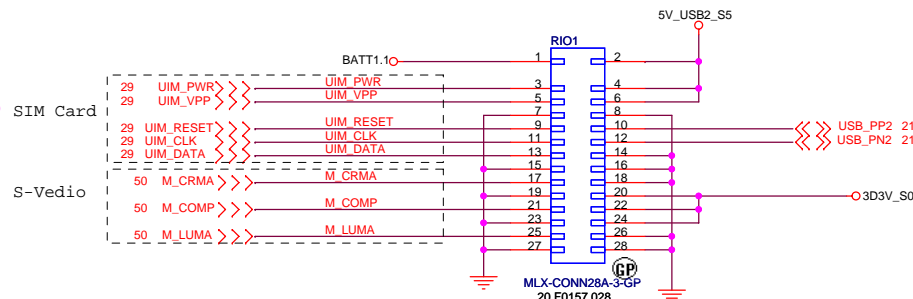
## To LED Board



## USB POWER



## To Right I/O Board



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Title

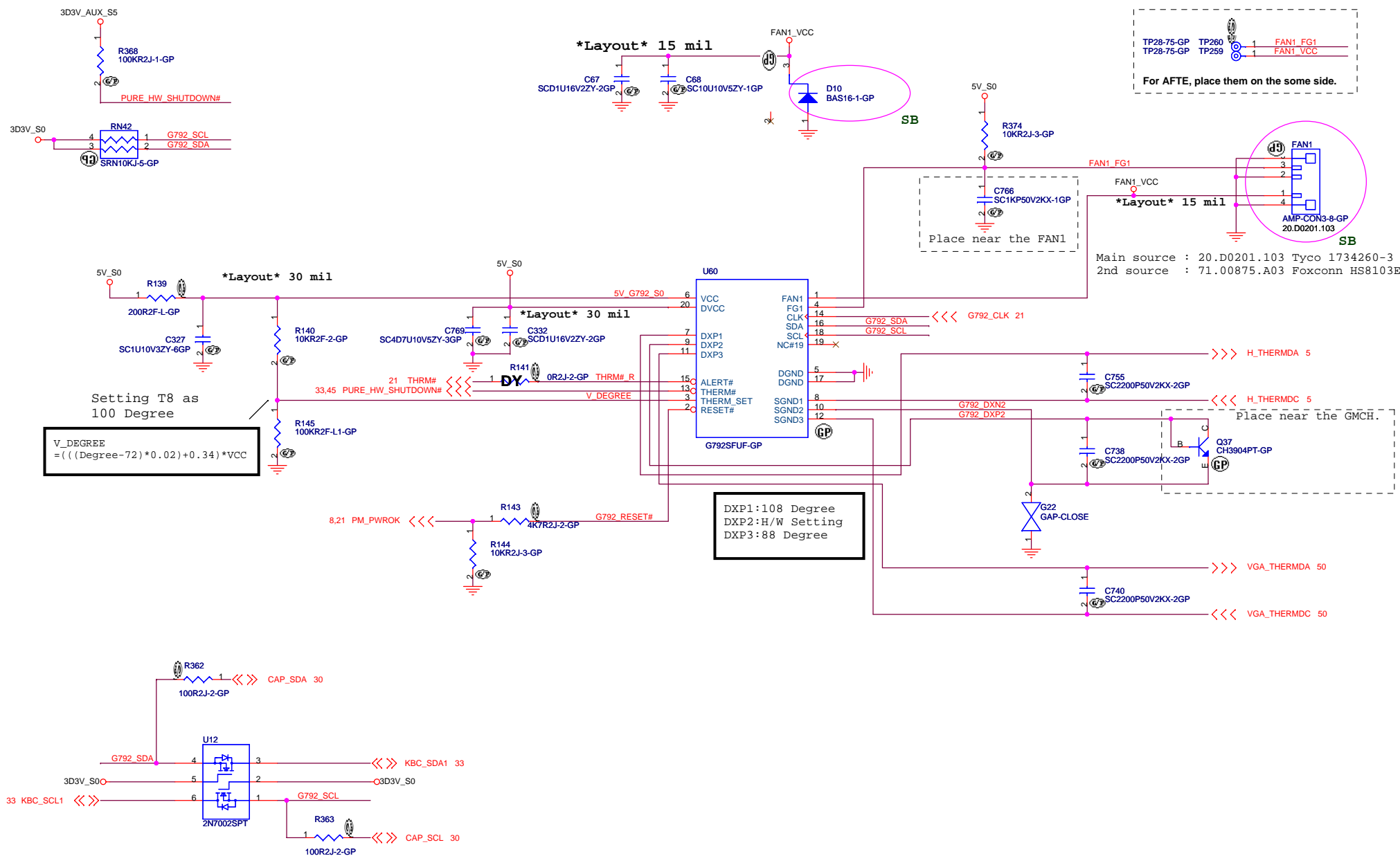
**Right I/O/ Power Dash**

Size A3 Document Number

**Hawke-Intel**

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Rev SC

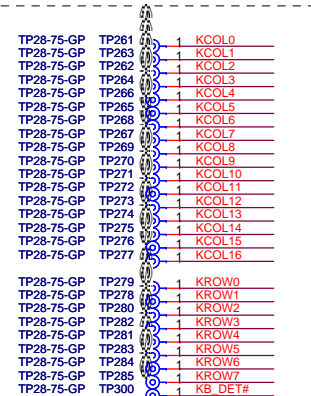
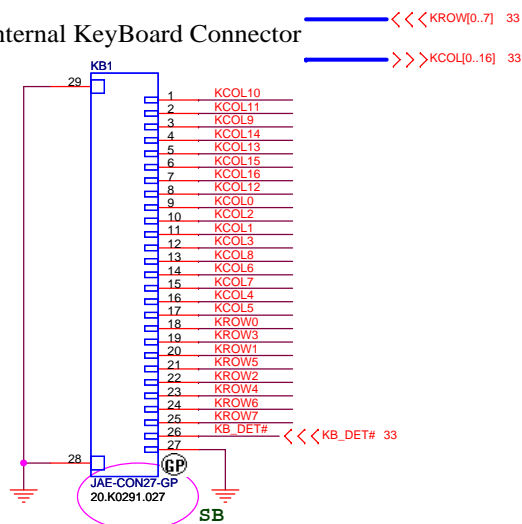


<Core Design>

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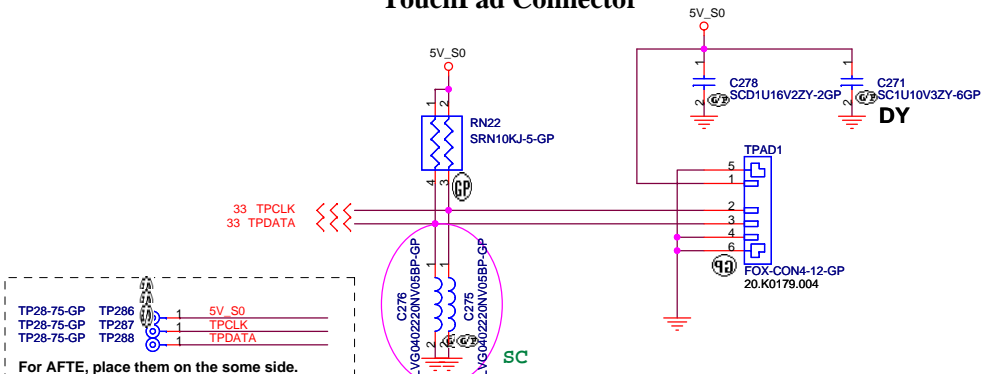
Title		
<b>Thermal/Fan Controller G792</b>		
Size	Document Number	Rev
A3	<b>Hawke-Intel</b>	<b>SC</b>
Date:	Friday, August 17, 2007	Sheet 35 of 57

## Internal KeyBoard Connector



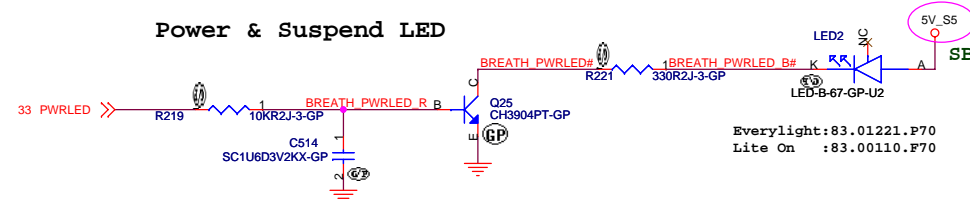
For AFTE, place them on the same side.

## TouchPad Connector



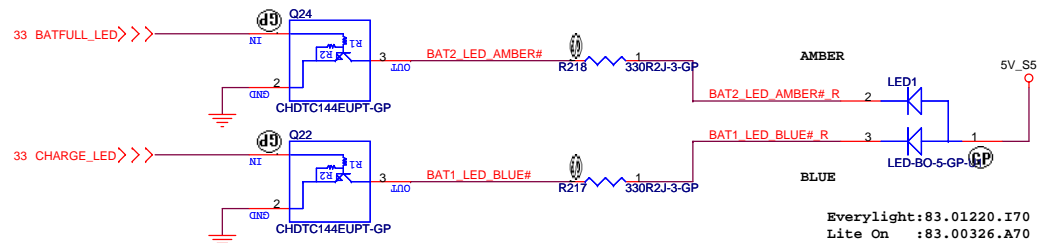
For AFTE, place them on the same side.

## Power & Suspend LED



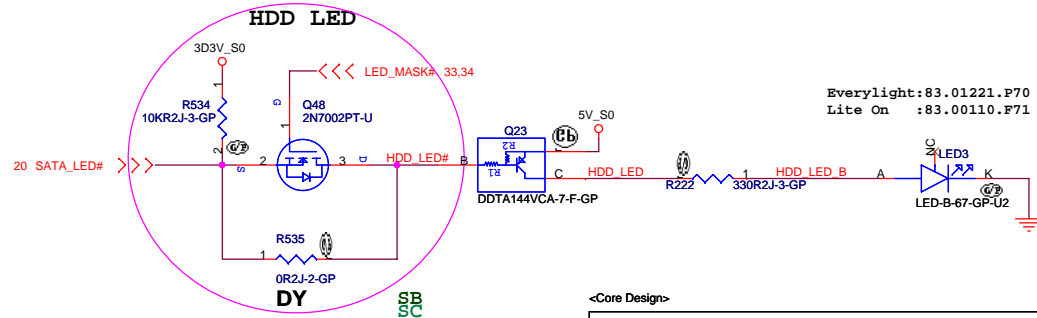
Everylight:83.01221.P70  
Lite On :83.00110.F70

## Battery LED



Everylight:83.01220.I70  
Lite On :83.00326.A70

## HDD LED



Everylight:83.01221.P70  
Lite On :83.00110.F71

## LED Board

LED NAME	ACTIVE SIGNAL
Power Button LED	PWR_BTN_LED
Instant Power Button LED	INST_ON_LED
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)
NUM LED	NUM_LED (from KBC)
SCRLK LED	SCRLK_LED (from KBC)
CAPS LED	CAP_LED (from KBC)

## Main Board

Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC)

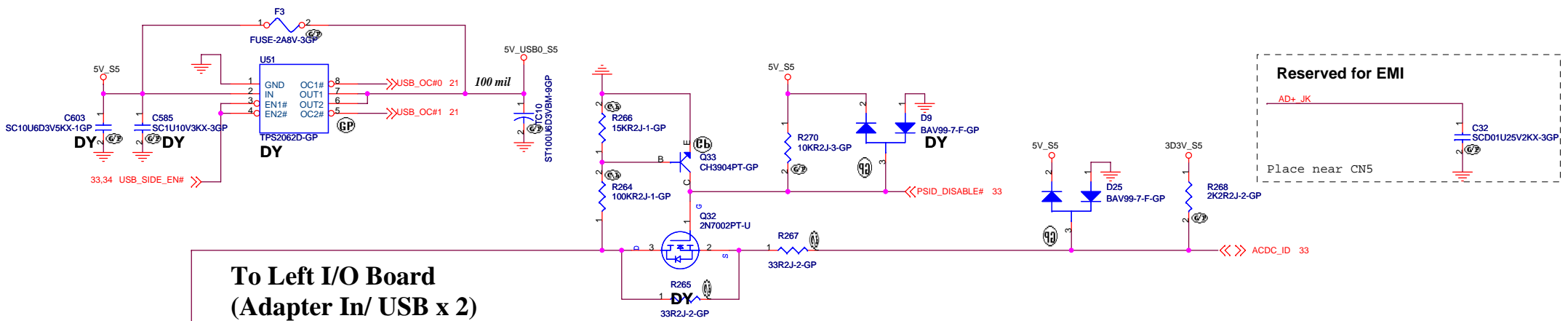
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<Core Design>

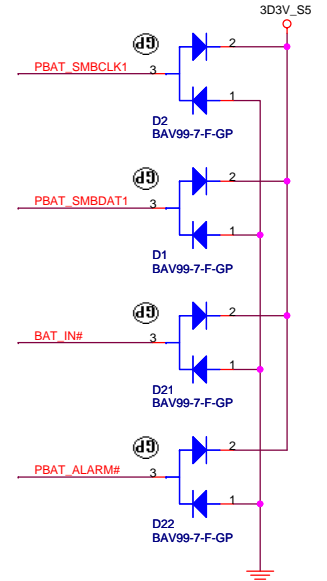
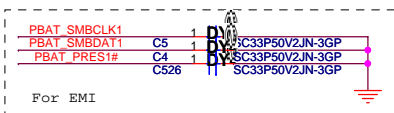
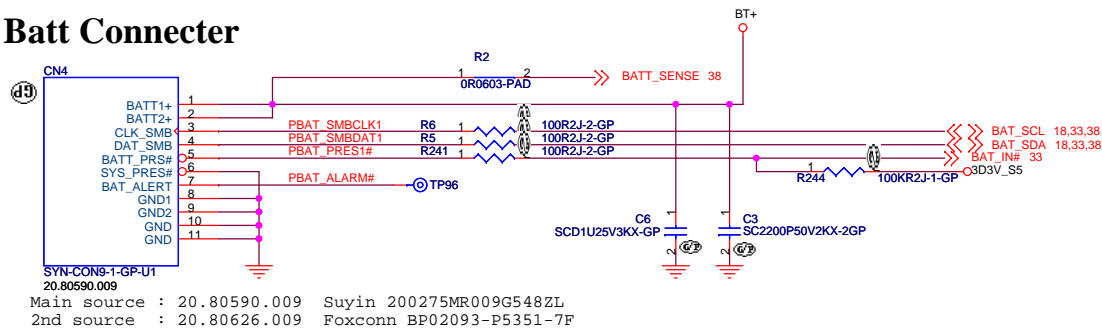
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title	KeyBoard/Touchpad	Rev	SC
Size A3	Document Number		
Date: Friday, August 17, 2007	Sheet 36	of	57

## USB POWER



## Batt Connector

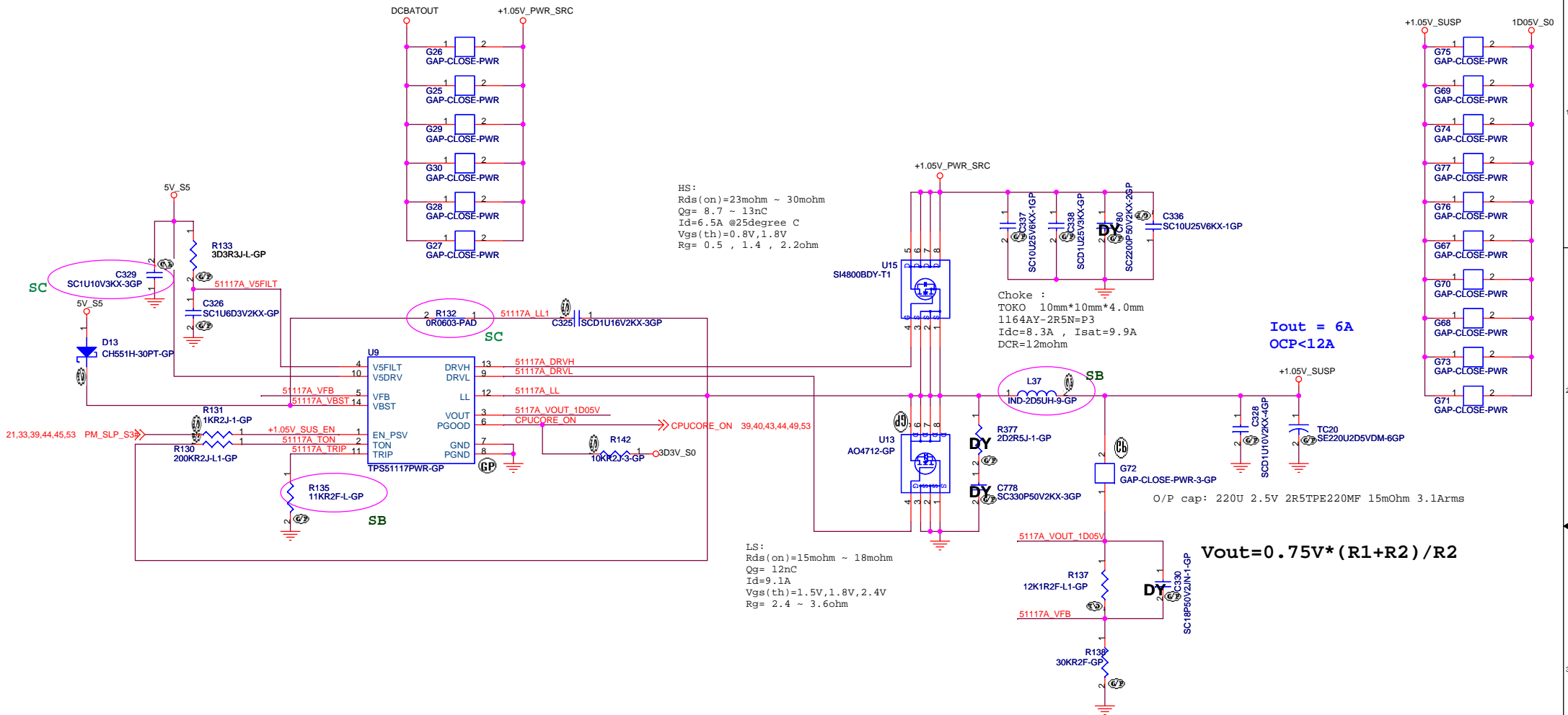




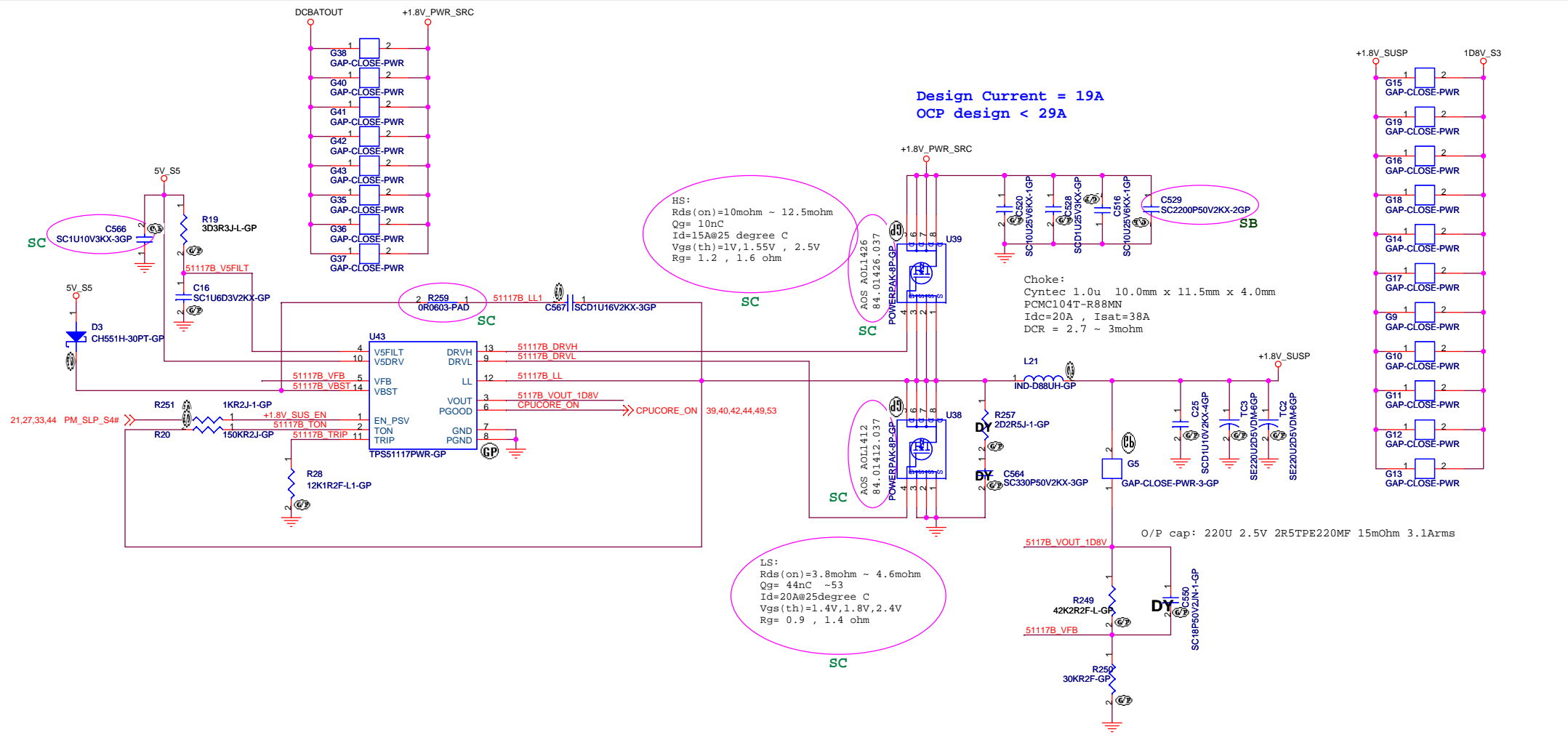






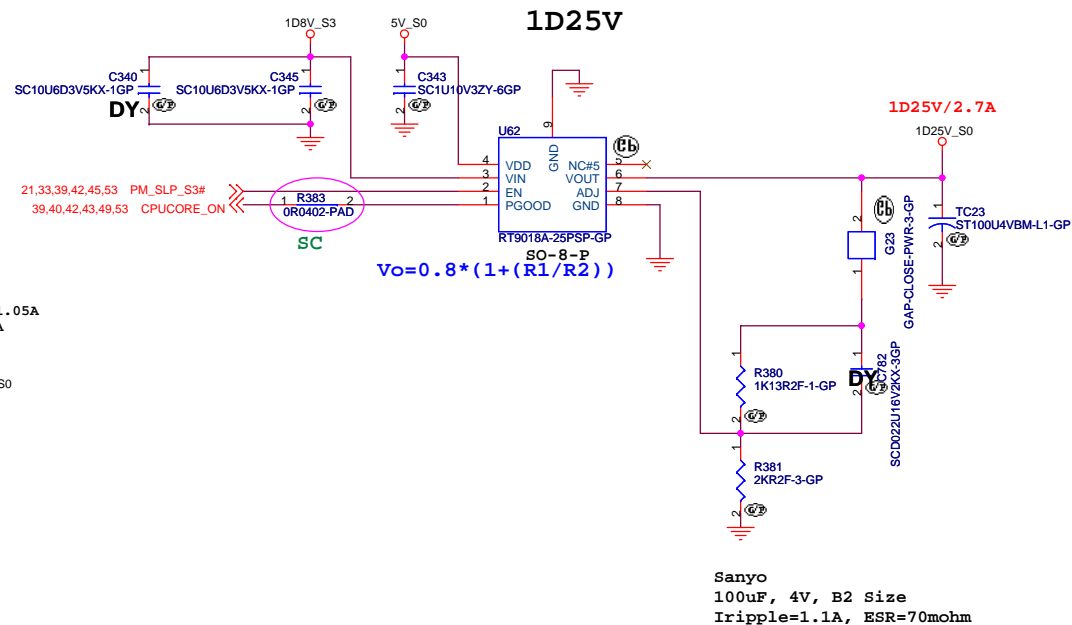
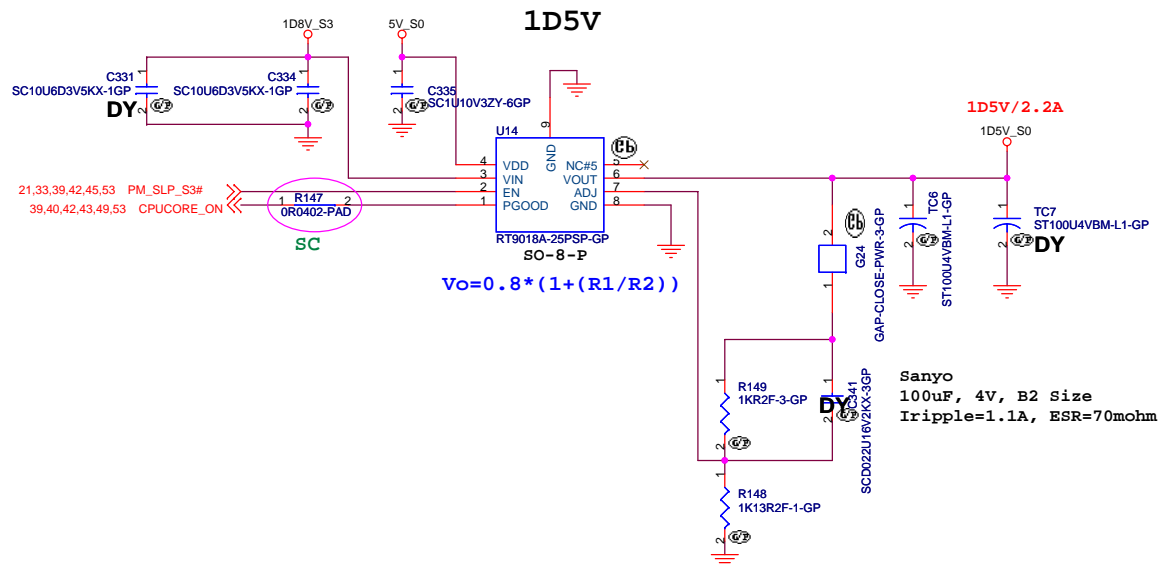


<Core Design>

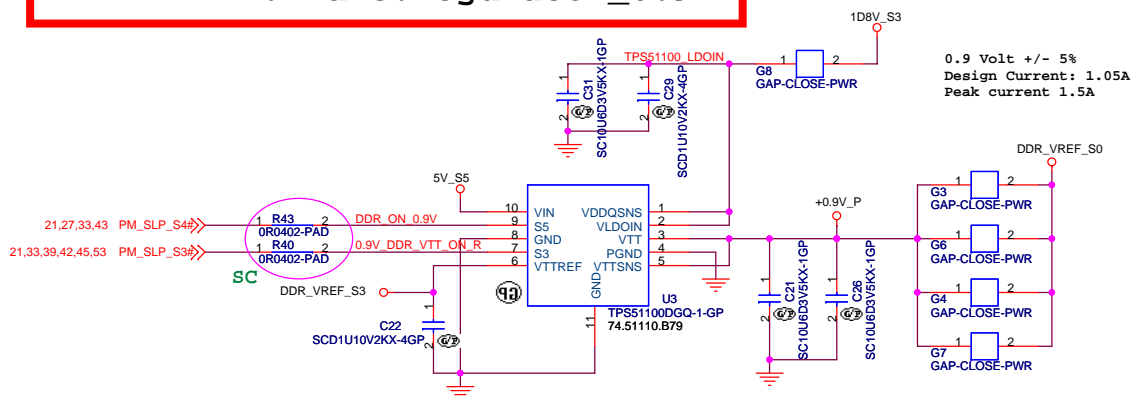


Design Current = 19A  
OCP design < 29A

$$V_{out} = 0.75V * (R1 + R2) / R2$$



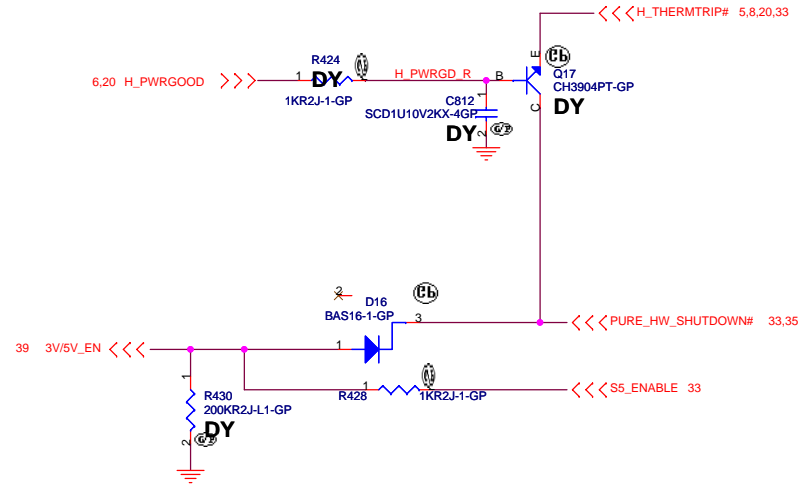
**SSID = PWR.Plane.Regulator\_0.9V**



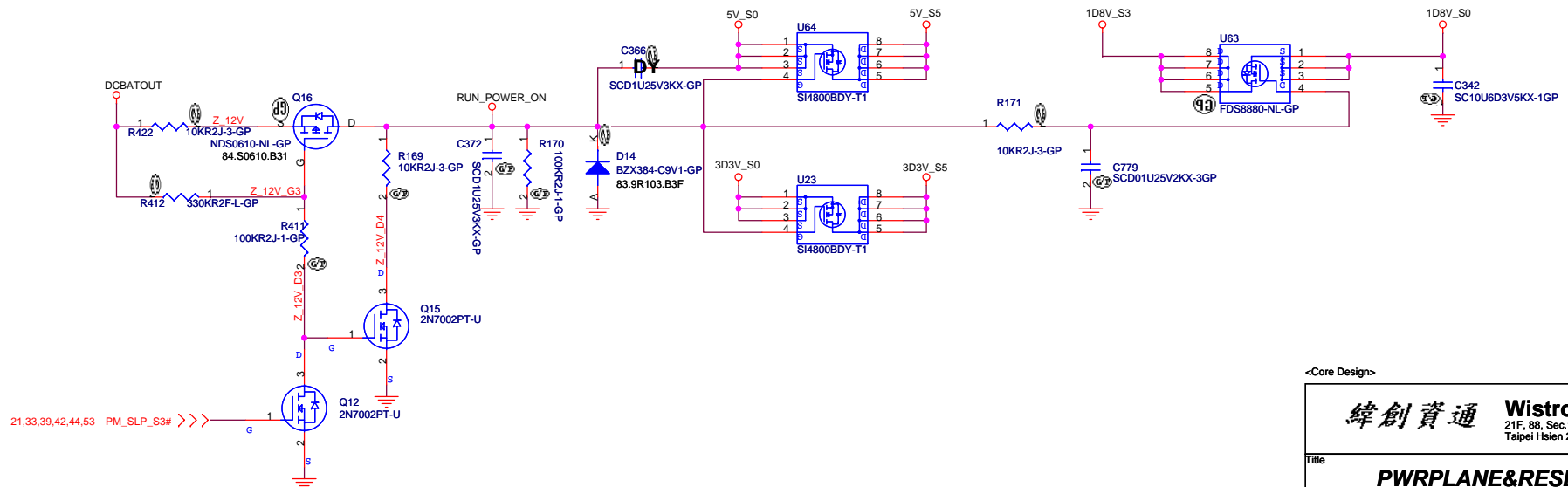
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
DC to DC 1D5V / 0D9V / 1D25V		
Size A3	Document Number	Rev
	Hawke-Intel	SC
Date: Friday, August 17, 2007	Sheet 44 of 57	



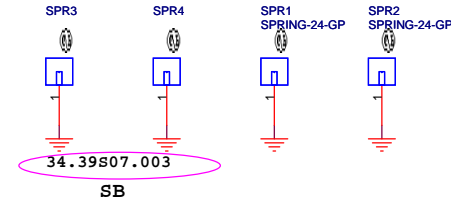
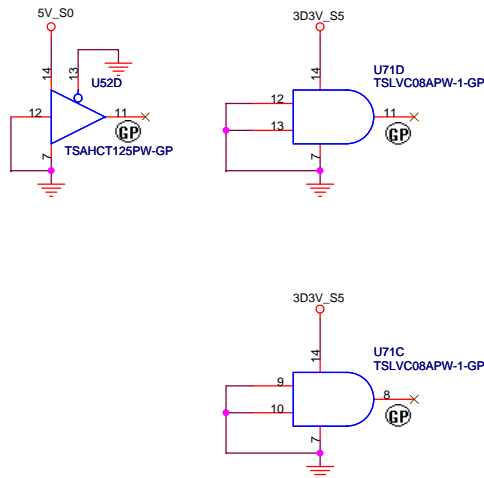
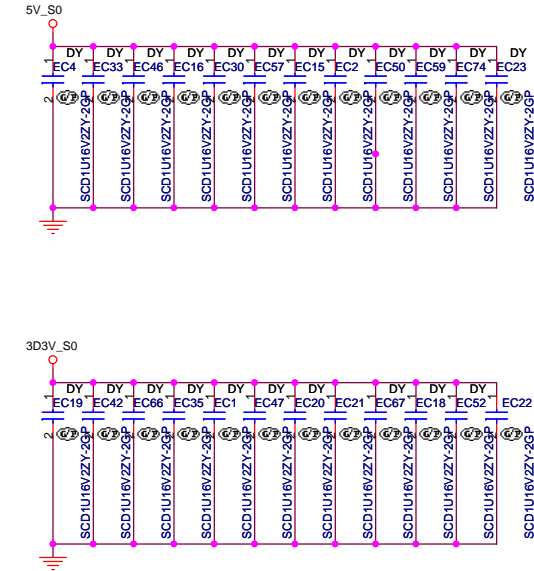
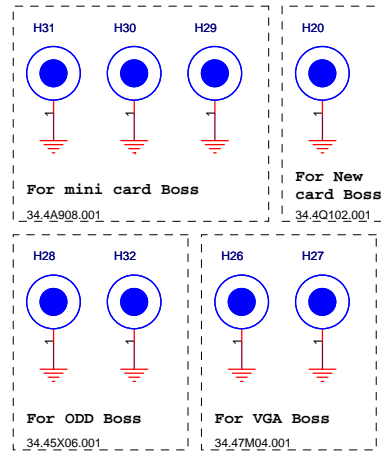
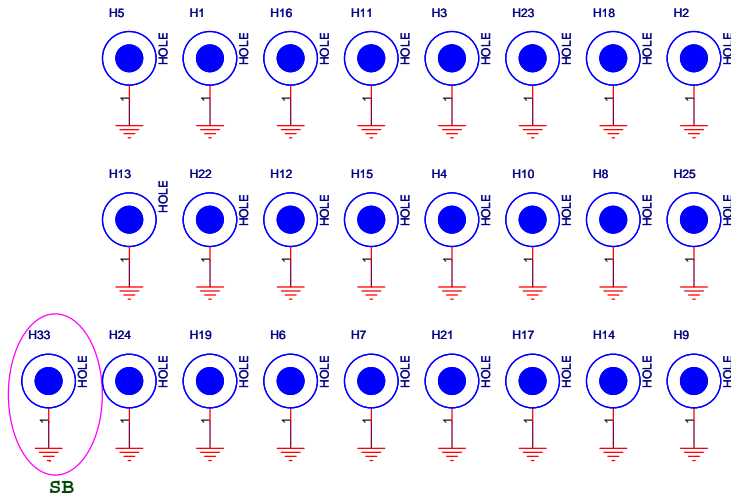
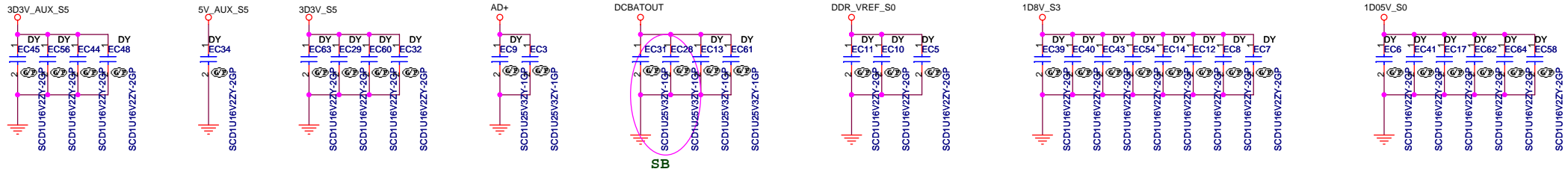
## Run Power



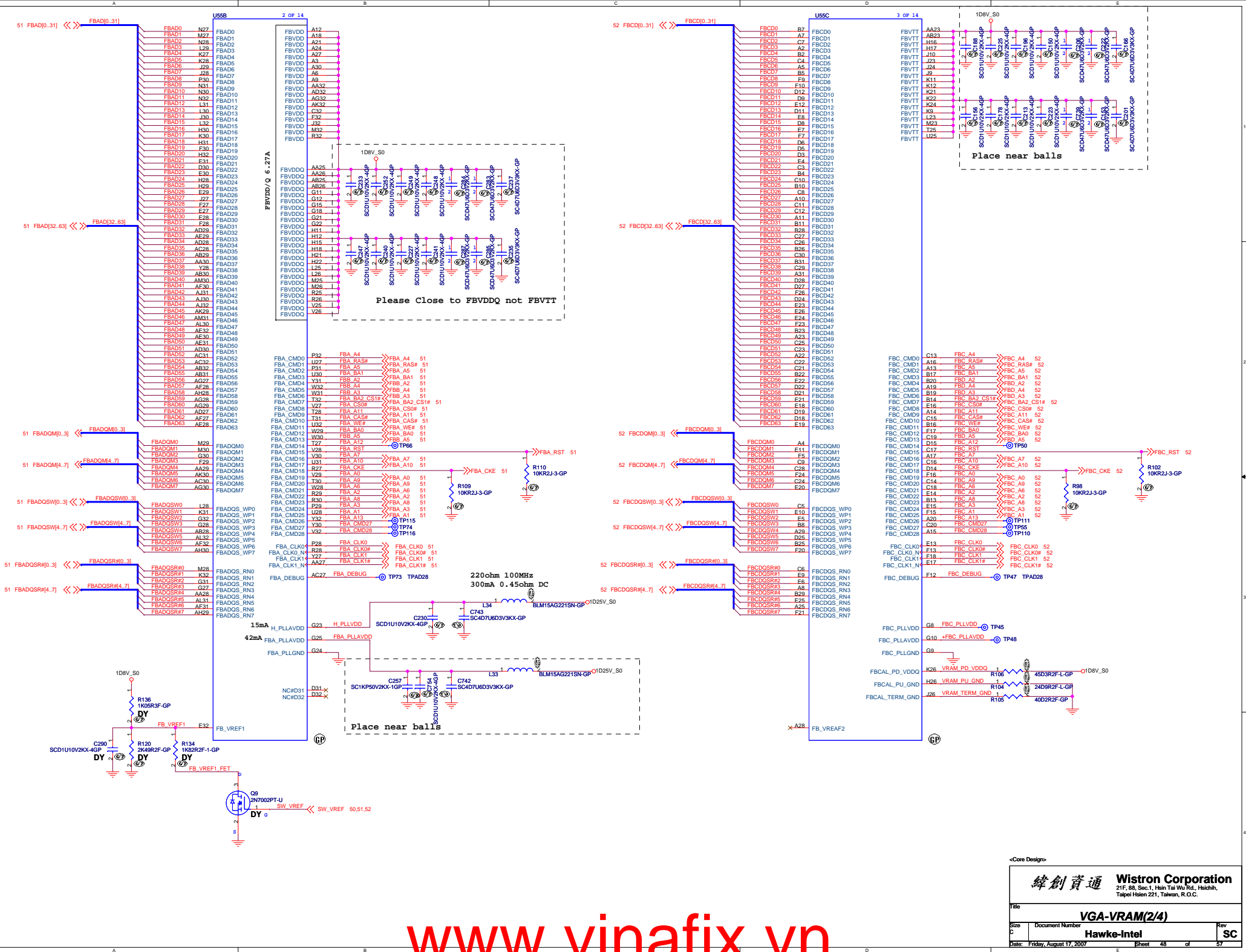
<Core Design>

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Title		<b>PWRPLANE&amp;RESETLOGIC</b>	
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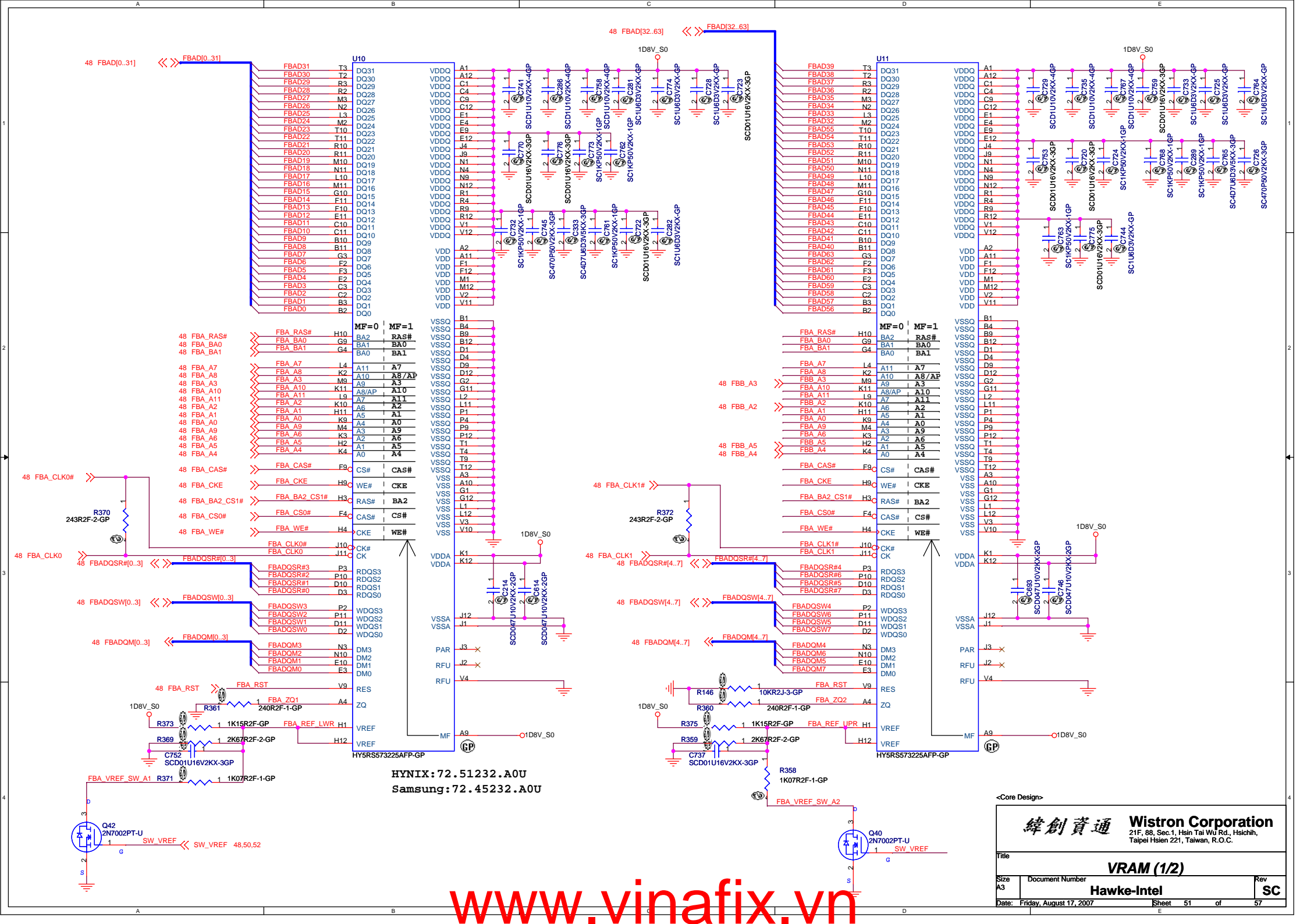












HYNIX: 72.51232.A0U  
Samsung: 72.45232.A0U

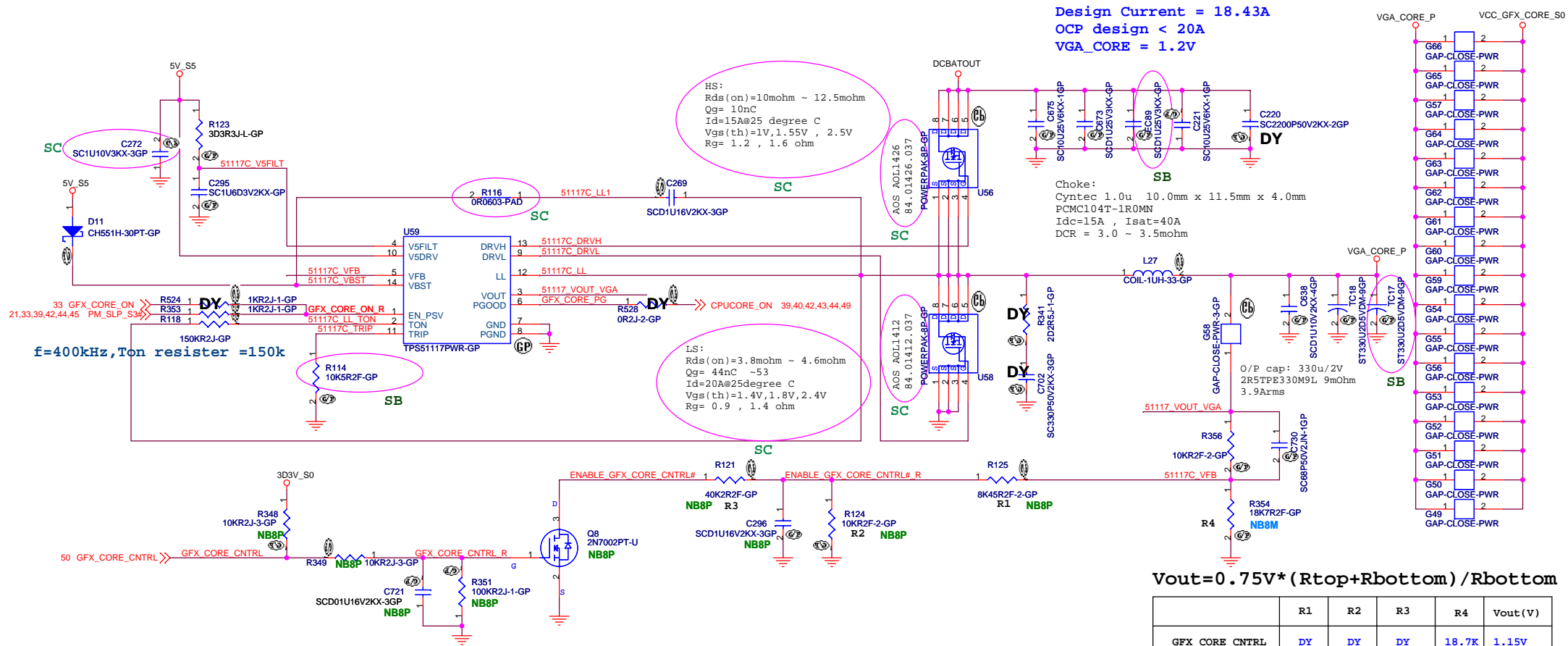
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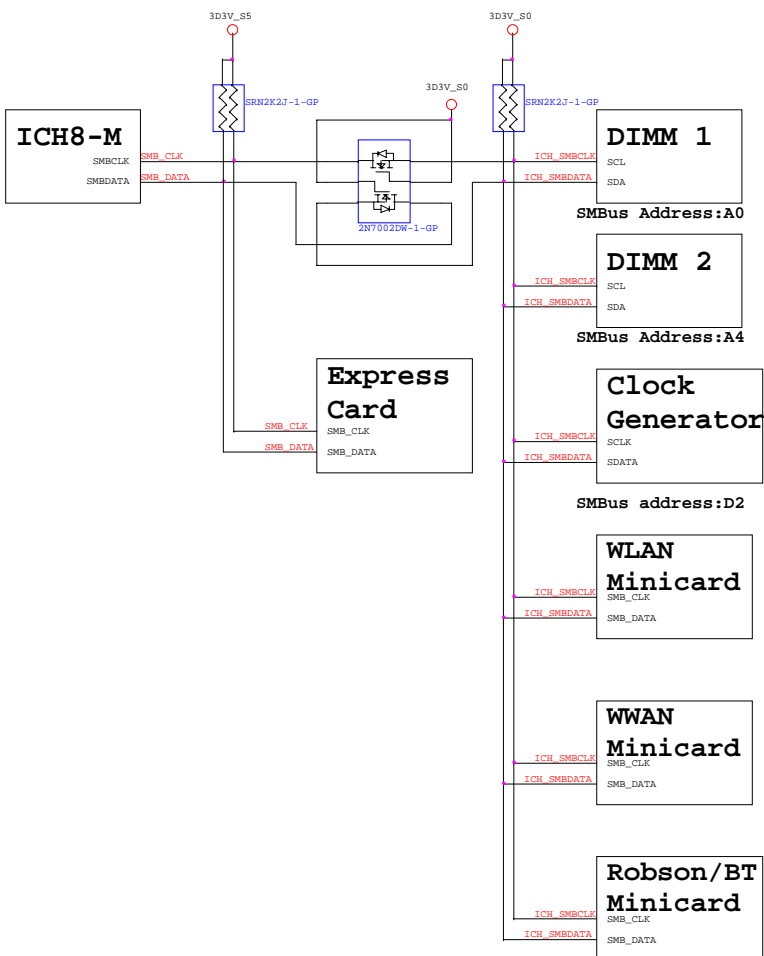
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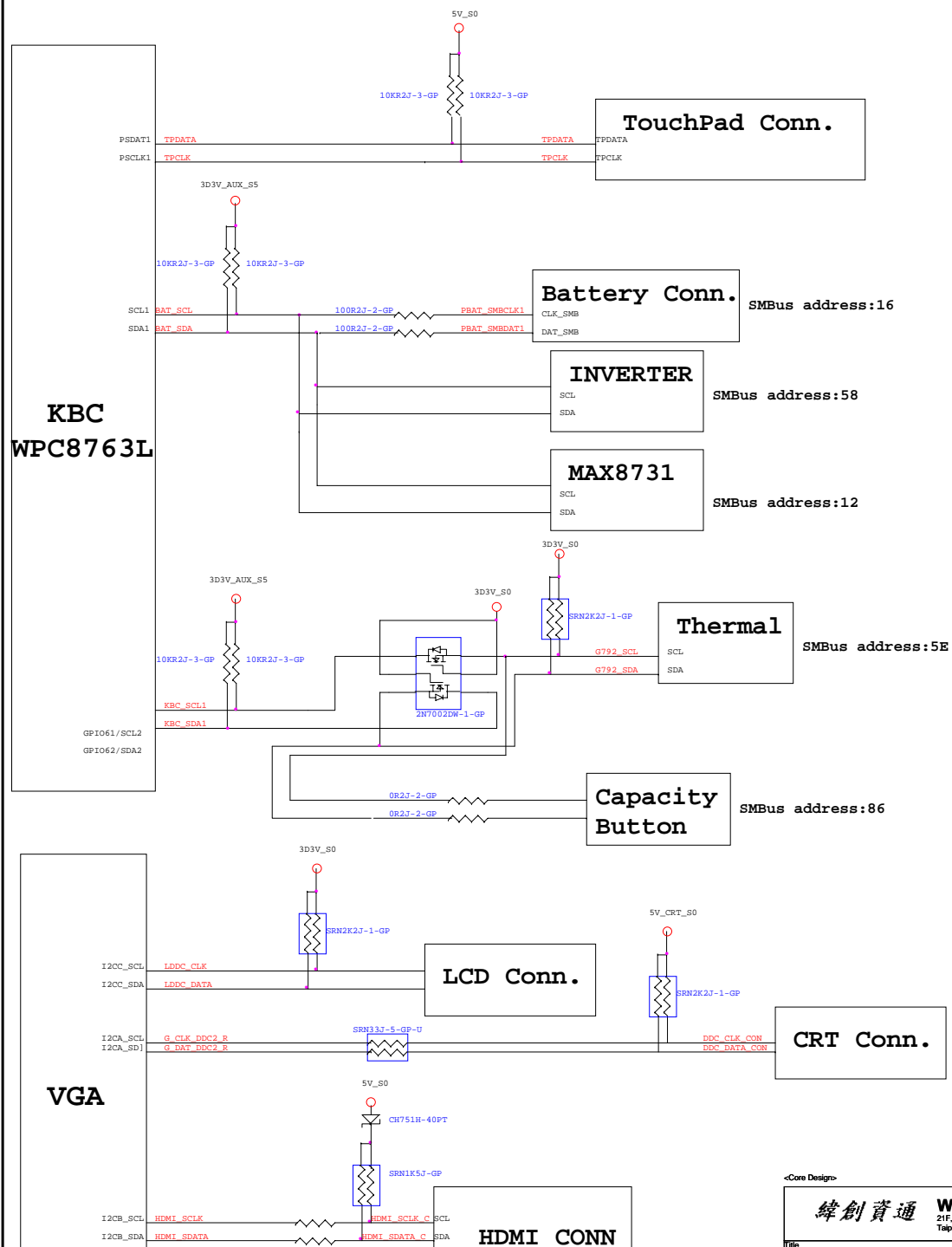




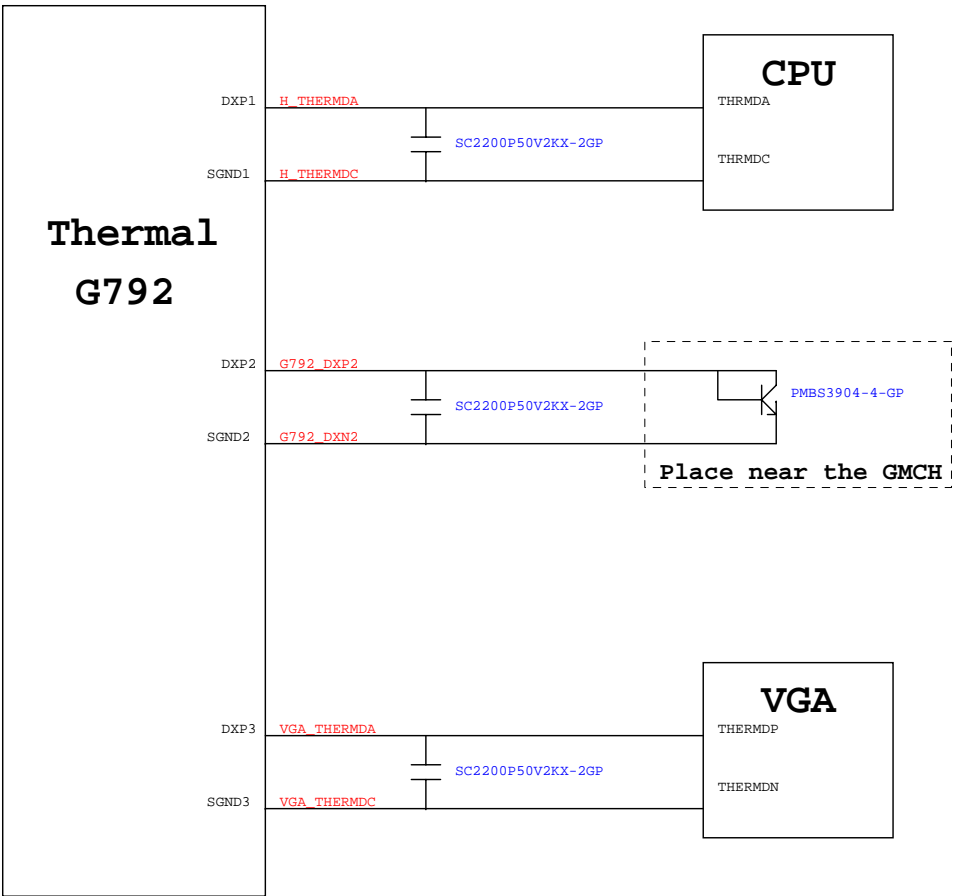
# ICH8 SMBus Block Diagram



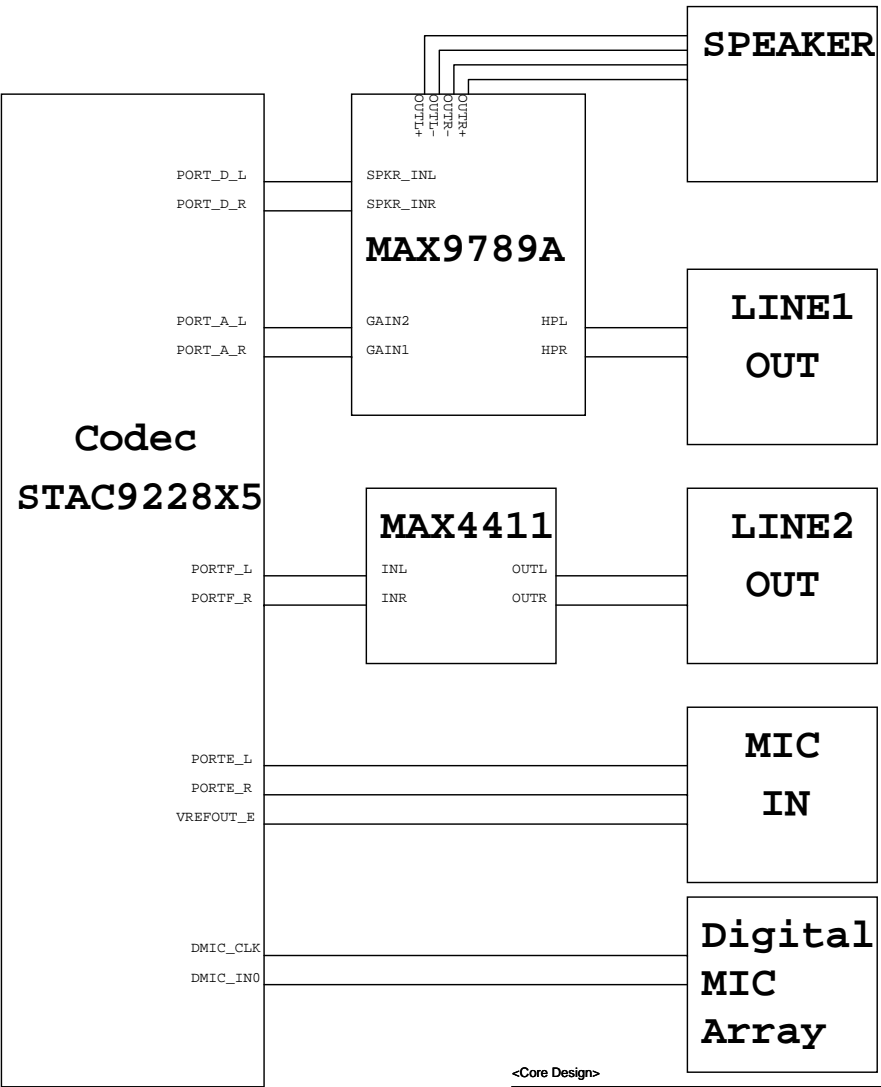
# KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/06	X00 to X01	1	4	Changed R431 from 10K ohm to 2.2K ohm.	Follow M08 design.	EE
		2	4	Changed X4's CL from 20pF to 10pF and changed C392 and C399 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		3	4	Changed RN27, RN28, RN29 and RN31 from 0 ohm to 22 ohm.	To solved these clock signals' Slew Rate are over spec.	EE
		4	18	Changed LVDS connector from 42-pin to 40-pin.	By ME suggestion.	ME
		5	18,33	Connected the LCD1 pin 3 to GND and connected pin 6 to WPC8763's GPIO05 (pin 108 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the LCD cable PAID.	EE
		6	18	Added EC75-EC78 near CAMERA1.	By EMC team suggestion.	EMC
		7	20	Change C354 and C355 from 15pF to 12pF and changed X1 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		8	21	Added R526 10K ohm between GPIO26 and 3D3V_S0, removed R404.	To solved 3D3V_S0 has leakage when S3 and S5.	EE
		9	21	Added the reserved Q47, D31, R530, R531 and R532.	For test EC_RMRST#_R circuit.	EE
		10	21	Changed R442 from 22.6 ohm to 20 ohm.	To sloved the left side USB ports and Camera USB's eye diagram fail.	EE
		11	23	Changed HDD connector.	By ME suggestion.	ME
		12	25	Changed 1394 connector.	To used reverse type by ME suggestion.	ME
		13	25	Changed X5's CL from 20pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		14	25	Removed R466, U26, R192 and D19, and connected the net MC_PWR_CTRL_0 to U25 pin 4.	For these materials are no used.	EE
		15	25	Populated C887, C888 and C894-C896.	By EMC team suggestion.	EMC
		16	26	Changed C387 and C390 from 27pF to 12pF.	By the Xtal vendor's FAE suggestion.	EE
		17	27	Changed RJ1 connector.	By ME suggestion.	ME
		18	30	Changed U61 from 8Mbits to 16Mbits SPI ROM.	By customer requirement.	EE
		19	30	Added EC79-EC82 near CAP1.	By EMC team suggestion.	EMC
		20	30	Added EC83-EC88 near BT1.	By EMC team suggestion.	EMC
		21	30	Added EC90-EC91 near CN2 (Biometric).	By EMC team suggestion.	EMC
		22	31	Changed C880 and C881 from 0402 size to 0603 size.	Follow Thurman design.	EE
		23	32	Swaped the nets AUD_HP1_OUT_R1, AUD_HP1_OUT_L1 with AUD_AMP_GAIN1, AUD_AMP_GAIN2.	To sloved the HP1 hadn't output.	EE
		24	32	Changed R211 and R212 from 100K ohm to 10M ohm.	To sloved the AUD_HP1_EN and AUD_HP2_EN volatge level lower than 2V.	EE
		25	33	De-pop R396 and populated R395.	To changed the MB version id to SB.	EE
		26	33	Changed R391 and R405 from 10K ohm to 100K ohm.	To sloved the INSTANT_BTN# and SNIFFER_PWR_SW# can't work.	EE
		27	33	Added R527 100K ohm between WLAN/BT_BTN# and 3D3V_AUX_S5.	To sloved the WLAN/BT_BTN# can't work.	EE
		28	33	Changed X2 package from DMX26S to SM-14J.	By the Xtal vendor's FAE suggestion.	EE
		29	33,36	Changed KB1 from 25-pin to 27-pin connector, connected the KB1 pin 27 to GND and connected pin 26 to WPC8763's GPI92 (pin 99 of U17) with 10K ohm pull up to 3D3V_AUX_S5.	Supported the KB cable PAID.	ME,EE
		30	33	Changed R408 and R389 from 10K ohm to 4.7K ohm.	By Vendor's FAE suggestion.	EE
		31	35	Changed FAN1 from 4-pin to 3-pin connector.	By ME suggestion.	ME
		32	36	Added R534, Q48 and R535 off SATA_LED# and Q23.	Supported the HDD LED is dim when sinffer switch press.	EE
		33	36	Connected LED2 pin A from 5V_S0 to 5V_S5.	To sloved the Power LED can't breath when system enter S3.	EE
		34	38	Changed C530 and C531 from 1206 size to 1210 size and populated C7.	To solved noise when battery full load.	Power
		35	39	Changed R477 from 12.1K ohm to 13.3K ohm and changed R468 from 12.1K ohm to 11.8K ohm.	To adjust 3.3V and 5V current limit by power team suggestion.	Power
		36	40	Changed R7 from 12.7K ohm to 11.8K ohm and changed R468 from 3.24K ohm to 3.65K ohm.	To adjust CPU Vcore current limit by power team suggestion.	Power
		37	42	Changed R135 from 12.1K ohm to 11K ohm .	To adjust 1.05V current limit by power team suggestion.	Power
		38	43	Populated C529.	By EMC team suggestion.	EMC
		39	46	Added more one hole H33.	By EMC team suggestion.	EMC
		40	46	Populated EC28 and EC31.	By EMC team suggestion.	EMC
		41	47	Added C900, C901, C904 10uF and TC26 100uF.	To sloved VGA Vcore had OVP when run 3Dmark.	Power
		42	53	Changed R135 from 12.1K ohm to 10.5K ohm .	To adjust CPU Vcore current limit by power team suggestion.	Power
		43	53	Added EC89 0.1uF between DCBATOUT and GND.	By EMC team suggestion.	EMC

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**HISTORY from X00 to X01**

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Document Number

**Hawke-Intel**

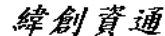
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2007/08/17	X01 to X02	1	4	Changed U22 from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	Changed clock gen symbol from ICS 9LPRS365BKLFT to Realtek RTM875M-606-LF.	EE
		2	15	Changed HDMI power rail from +5V_HDMI to 5V_S0.	Follow Thurman design.	EE
		3	17	Populated D4, D5, D6, D7 and D8.	By NV GPU ESD requirement.	EMC
		4	17	Changed L1, L2 and L4 from BLM18BA100SN1 to BLM18BB470SN1	To solve the ring on RGB singnal.	EE
		5	18,33	Added D32, connected pin 1 to LCDVDD_TST_EN, pin 2 to LCDVDD_EN and pin 3 to ENVDD. Changed R276 from 0 to 100k ohm and changed R276.1 to GND	Added LCDVDD_TST_EN from U17.27 to control U53.3	EE
		6	18	Disconnted LCD1 pin 3 and pin 10	To prevent the power short to GND.	EE
		7	21	Added R542 for ECSCI# need to pull up 3D3V_S0	To solve one of CPU core always loading 100%.	EE
		8	27	Added EC92 22pF between NEWCARD_CLKREQ# and GND	By EMC team suggestion.	EE
		9	27	Added note for transformer source part number.	By EMC team suggestion.	EE
		10	29	1.Changed D20 to U73 for Bluetooth Action circuit. 2.Reserved U73, R193 and R195, populated R194.	1.It can be used both BT module and BT mini-card. 2.Just keep BT module now.	EE
		11	29, 33	Connect MINI2 pin 20 to U17.24 (GPO47 of KBC).	Changed WWAN enable WiFi RF controlled by another GPIO pin (U17.24 is GPO47 of KBC).	EE
		12	30, 33	Rename SNIFFER_YELLOW# to SNIFFER_YELLOW, SNIFFER_BLUE# to SNIFFER_BLUE.	These pins are High active.	EE
		13	30	Disconnted SNIFFER_BD1 pin 8 and CAP1 pin 7.	To prevent power short to GND.	EE
		14	30	Changed EC90 and EC91 from 22pF to MLVG0402220NV05BP.	By EMC team suggestion.	EMC
		15	32	Populated EC24, EC25, EC26 and EC27 and change to 1000pF.	By EMC team suggestion.	EMC
		16	32	Changed Q45 to U47 and added R543.	To add AUD_SPK_ENABLE# controlled by AMP_MUTE#.	EE
		17	32	Changed R197 from 0 ohm to 100K ohm and pull up to +5V_SPK_AMP, dispopulated R505 and populated R213.	To solve HP1, HP2 and Speaker have "BoBo" noisy when power on, off, enter S3.	EE
		18	33	Populated R396 and R398, dispopulated R395 and R399.	Change Board ID to version SC.	EE
		19	36	Populated Q48 and R534, dispopulated R535.	HDD LED should be dim when power on by Sniffer button.	EE
		20	36	Changed C275 and C276 from reserved 33pF to MLVG0402220NV05BP, and populated them	By EMC team suggestion.	EMC
		21	36	Changed KB EMI caps from 220pF to 180pF.	To solved the word has repeat symptom when key-in.	EE
		22	38	The U42 and U44 were swap the main source and 2nd source.	To prevented used AO4468 that SI4800BDY 2nd source on charger H/S and L/S MOS.	EE
		23	39	Populated R485 and dispopulated R489.	To changed 3V and 5V PWM to Skip mode.	EE
		24	42, 43, 53	Changed C329, C566 and C272 rated voltage from 6.3V to 10V.	For derating issues by power team requirment.	EE
		25	43, 53	Change the U56 and U39 from 2nd source to main source, and swap the U38 and U58's the main source and 2nd source	To combined U39 and U56 material item of BOM with CPU H/S MOS (U4 and U35).	EE
		26	20	Changed C354 and C355 from 12pF to 8.2pF.	For Negative Resistance of X1 isn't enough.	EE
		27	33	Changed C350 and C351 from 15pF to 10pF.	For Negative Resistance of X2 isn't enough.	EE

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